

## Digital Blocks Announces the DB-I2C Controller IP Core with the availability of Master-Slave, Master, and Slave Versions for the AMBA 2.0 APB Interconnect

*Specifically targeted for Embedded Processor designs with AMBA 2.0 APB Bus requirements, the DB-I2C offers a variety of performance levels versus VLSI footprint tradeoff options.*

**GLEN ROCK, New Jersey, December 20, 2007** – Digital Blocks, a leading developer of silicon-proven semiconductor Intellectually Property (IP) soft cores for embedded processor and video system designers, today announces the DB-I2C Controller IP Core. The DB-I2C IP Core targets systems-on-chip (SoC) ASSP, ASIC, and FPGA designs containing ARM embedded processors and the AMBA 2.0 APB on-chip bus, as well as other processors that support the APB bus.

The DB-I2C IP Core is offered in three versions:

<b>Model Number</b>	<b>Description</b>
DB-I2C-MS-APB	Provides both Master and Slave function with optional parameterized FIFO for high performance designs.
DB-I2C-M-APB	Master only function with optional FIFO for smaller VLSI footprint.
DB-I2C-S-APB	Slave only function with optional FIFO or register bank with auto-increment addressing mode.

### Price and Availability

The DB-I2C is available immediately in synthesizable Verilog or VHDL, along with synthesis scripts, a simulation test bench with expected results, datasheet, and user manual. For further information, product evaluation, or pricing, please visit Digital Blocks at <http://www.digitalblocks.com>

### About Digital Blocks

Digital Blocks designs silicon-proven IP cores for technology systems companies, reducing customer's development costs and significantly improving their time-to-volume goals. Digital Blocks is located at 587 Rock Rd, Glen Rock, NJ 07452 (USA).

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