General Description

The Digital Blocks DB-I2C-M-AVLN Controller IP Core interfaces a microprocessor via the Avalon Bus to an I2C Bus. The I2C is a two-wire bidirectional interface standard (SCL is Clock, SDA is Data) for transfer of bytes of information between two or more compliant I2C devices, typically with a microprocessor behind the master controller and one or more slave devices.

The DB-I2C-M-AVLN is a Master I2C Controller that controls the Transmit or Receive of data to or from slave I2C devices. In an Altera FPGA, typically, the microprocessor is a NIOS II processor, but can be any FPGA embedded processor. Figure 1 depicts the system view of the DB-I2C-M-AVLN Controller IP Core embedded within an FPGA integrated circuit device.

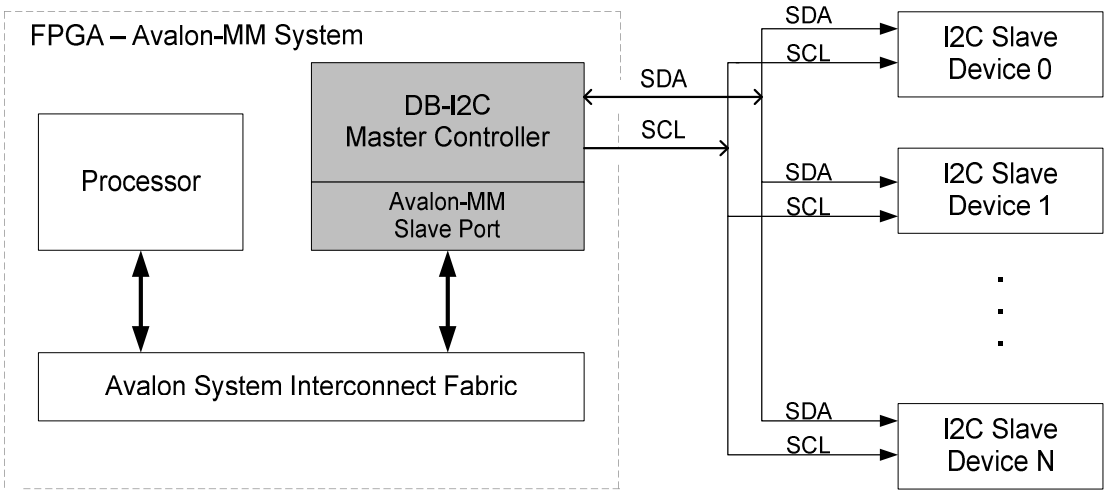

Figure 1: DB-I2C-M-AVLN Controller – System Diagram

The DB-I2C-M-AVLN Controller IP Core targets embedded processor applications with high performance algorithm requirements. While most I2C controllers require high processor interaction involvement, the DB-I2C-M-AVLN contains a parameterized FIFO and Smart Control for the processor to off-load the I2C transfer to the DB-I2C-M-AVLN Controller. Thus, while the DB-I2C-M-AVLN is busy, independently controlling the I2C Transmit or Receive transaction of data, the processor can go off and complete other tasks. Note that the Master only capability of the DB-I2C-M-AVLN adds to its small VLSI footprint requirements.

Features

- I2C Master only with Parameterized FIFO:
  - Targets embedded processors with high performance algorithm requirements, by independently controlling the Transmit or Receive of bytes of information:
    - For Transmits, the processor writes the Slave Address & bytes of information into the FIFO, sets a start control bit, and waits for an interrupt or polls a status bit signaling completion
    - For Receive, the processor writes the Slave Address into the DB-I2C-M-AVLN, sets a start control bit, and waits for an interrupt or polls a status bit signaling completion. The processor then reads the bytes of information from the FIFO.
  - Small VLSI footprint.
- Master Controller Modes:
  - Master – Transmitter
  - Master – Receiver
- Parameterized 8-bit FIFO for higher performance. Optional 16 or 32-bit processor interface.
- Supports two I2C bus speeds:
  - Standard mode (100 Kb/s)
  - Fast mode (400 Kb/s)
- 7 sources of internal interrupts with masking control
- Compliance with Altera Avalon and I2C specifications:
  - Compliance with Avalon Memory Mapped Interface Specification (MNL-AVABUSREF-3.2)
  - Philips/NXP – The I2C-Bus Specification, Version 2.1, January 2000
- Fully-synchronous, synthesizable Verilog or VHDL RTL core, with rising-edge clocking, no gated clocks, and no internal tri-states, for easy integration into FPGA or ASIC design flows.

Pin Description

In addition to the Avalon Slave Bus interfaces, which include the input CLOCK and RESET signals and the output INTR (interrupt) signal, the I2C interface signals are listed in Table 1.

Name	Type	Description
I2C Bus interface		
SDAi	Input	Serial Data
SDAo	Output	Serial Data
SCLo	Output	Serial Clock Line

Table 1: DB-I2C-M-AVLN – I/O Pin Description

Verification Method

The DB-I2C-M-AVLN Controller IP Core contains a test suite with Avalon Bus functional models that program the DB-I2C-M-AVLN control & status registers, generates & sends I2C data, monitors the I2C bus protocol, and checks expected results.

The DB-I2C-M-AVLN Controller IP Core has been verified as follows:

- Instantiated within an FPGA, controlled by a NIOS II processor, and communicating with (1) a merchant semiconductor device containing an I2C Slave bus interface; and (2) an ASIC containing an I2C Slave bus interface

Customer Evaluation

Digital Blocks offers a variety of methods for prospective customers to evaluate the DB-I2C-M-AVLN. Please contact Digital Blocks for additional information.

Deliverables

The DB-I2C-M-AVLN is available in synthesizable RTL Verilog or VHDL or a technology-specific netlist for FPGAs, along with synthesis scripts, a simulation test bench with expected results, datasheet, and user manual.

The DB-I2C-M-AVLN comes along with example C code software for controlling Transmit and Receive Transactions in the Eclipse-based Nios® II Integrated Development Environment (IDE).

The DB-I2C-M-AVLN comes along with Altera SOPC Builder components, for easy interface to the Avalon Bus, and thus the NIOS II processor.

Implementation Results

Implementation results for the DB-I2C-M-AVLN IP Core for a variety of Altera FPGA devices are listed in Table 2:

Altera Device	Utilization		Memory Bits	M4K / M9K BLK Memory	I/O	Fmax (MHz)
	LEs	ALUTS				
Cyclone II EP2C5-C7	292	-	128[1]	1[1] (M4K)	2[2]	160[3]
Cyclone III EP3C5-C6	297		128[1]	1[1] (M4K)	2[2]	215
Stratix III EP3SL50-C2	-	249	128	1 (M9K)	2	364

[1] FIFO parameter set to 16 words x 8 bits. Single M4K memory block can support 512 x 8 FIFO
[2] I2C signals at FPGA I/O, SCL / SDA. Additional on-chip Avalon Bus signals to processor
[3] Input clock from Avalon Bus. SCL clock output programmable divide down to 100 KHz / 400 KHz, according to I2C Bus Standard

Table 2: DB9000AVLN – Altera FPGA Utilization & Performance

Ordering Information

Please contact Digital Blocks for additional technical, pricing, evaluation, and support information.

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