

## Digital Blocks Announces I2C-Master Controller IP Core Family with the availability of the DB-I2C-M for the ARM AMBA 2.0 APB and Altera NIOS II Avalon Interconnects

*The DB-I2C-M targets High-Performance Embedded Processor designs requiring a Smart I2C Controller in a small VLSI footprint.*

**GLEN ROCK, New Jersey, July 18, 2008** – Digital Blocks, a leading developer of silicon-proven semiconductor Intellectually Property (IP) soft cores for embedded processor and video system designers, today announces the DB-I2C-M Controller IP Core. The DB-I2C-M IP Core targets systems-on-chip (SoC) ASSP, ASIC, and FPGA designs containing embedded processors with high performance algorithm requirements.

The DB-I2C-M contains a parameterized FIFO, enabling the processor to off-load the I2C transfers to the DB-I2C-M Core. This frees-up the processor for other useful algorithmic tasks. In addition, the DB-I2C-M Core offers the I2C Master only function, providing a smaller VLSI footprint for a processor with slave-only I2C devices to control.

The DB-I2C IP Core is offered in two versions:

Model Number	Description
DB-I2C-M-APB	I2C Master only function with parameterized FIFO for high performance ARM processor designs.
DB-I2C-M-AVLN	I2C Master only function with parameterized FIFO for high performance Altera NIOS II processor designs.

### Price and Availability

The DB-I2C-M is available immediately in synthesizable Verilog or VHDL, along with synthesis scripts, a simulation test bench with expected results, datasheet, and user manual. For further information, product evaluation, or pricing, please visit Digital Blocks at <http://www.digitalblocks.com>

### About Digital Blocks

Digital Blocks designs silicon-proven IP cores for technology systems companies, reducing customer's development costs and significantly improving their time-to-volume goals. Digital Blocks is located at 587 Rock Rd, Glen Rock, NJ 07452 (USA).

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