General Description

The DB-I2C-S-SCL-CLK is an I^2C Slave Controller IP Core focused on low power, low noise ASIC / ASSP designs requiring the configuration & control of registers with no free running clock. The DB-I2C-S-SCL-CLK processes the I^2C protocol & physical layers, and receives & transmits bytes with respect to the I^2C payload to / from User Registers within an ASIC / ASSP / FPGA device.

The DB-I2C-S-SCL-CLK Controller implements the Slave-Transmit and Slave-Receive protocol according to the Philips I2C-Bus Specification, Version 2.1 as well as the updated NXP UM10204 Rev 6 – 4 April 2014 Specification.

Figure 1 depicts the system view of the DB-I2C-S-SCL-CLK Controller IP Core embedded within an ASIC, ASSP or FPGA device. The DB-I2C-S-SCL-CLK Controller receives and transmits data with respect to an external I2C Master Controller. The DB-I2C-S-SCL-CLK internally interfaces to User Registers.

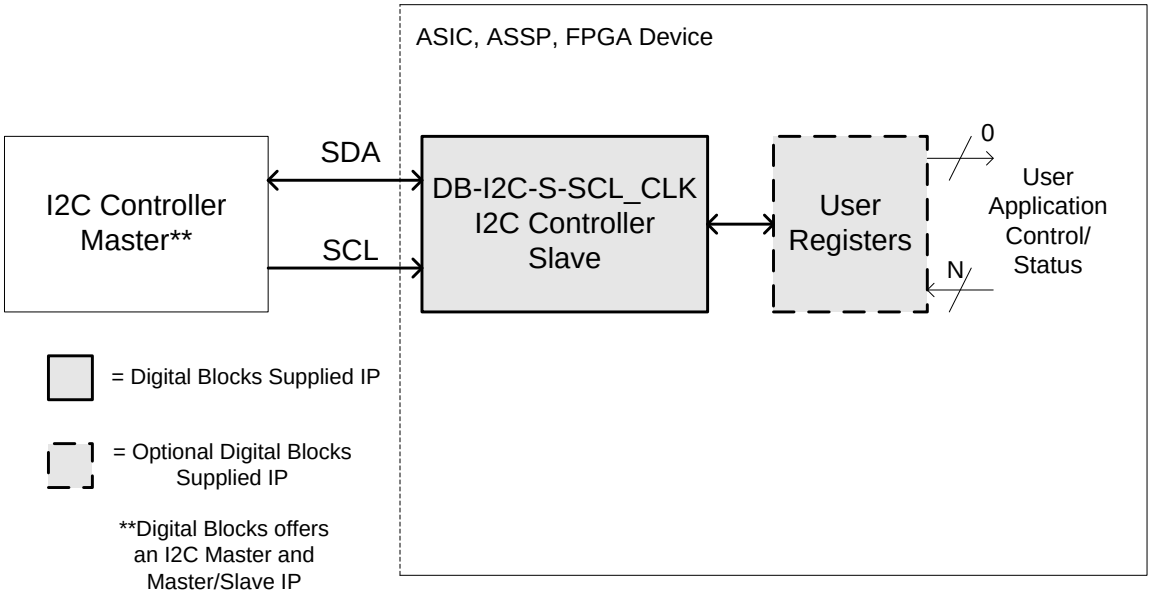

Figure 1: DB-I2C-S-SCL-CLK Controller - System View

Features

- Slave I^2C Controller Modes:
  - Slave – Transmitter
  - Slave – Receiver
- Supports following I2C bus speeds:
  - Hs-Mode (3.4+ Mb/s)
  - Ultra Fast-Mode (5 Mb/s)
  - Fast Mode Plus (1 Mb/s)
  - Fast Mode (400 Kb/s)
  - Standard Mode (100 Kb/s)
- I2C compliant features:
  - Repeated Start, 7/10-bit addressing, General Call, SCL Low Wait States
- SCL Clock only for low power, low noise applications requiring configuration & management of User Registers
- Compliance with I2C specifications:
  - Philips/NXP – The I2C-Bus Specification, Version 2.1, January 2000
  - NXP UM10204 Rev 6 – 4 April 2014
- Fully-synchronous, synthesizable Verilog RTL core. Easy integration into FPGA or ASIC design flows.

Pin Description

The DB-I2C-S-SCL-CLK I2C Slave Controller interface signals are listed in Table 1. Note that a bi-directional driver is available for SDAI / SDAO.

Name	Type	Description
I2C Bus Interface		
SDAI	Input	Serial Data
SDAO	Output	Serial Data
SCLI	Input	Serial Clock Line
User Register Interface		
Please contact Digital Blocks for more information		

Table 1: DB-I2C-S-SCL-CLK – I/O Pin Description

Verification Method

The DB-I2C-S-SCL-CLK Controller IP Core contains a verification test suite that generates & sends I2C transactions, monitors the I2C bus protocol, and checks expected results.

The DB-I2C-S-SCL-CLK Controller IP Core has internally been verified as follows:

- Instantiated within an FPGA, and communicating with NXP I2C Master IP Controller.
- Instantiated within an FPGA, and communicating with Digital Blocks I2C Master IP Controller, and A NIOS II processor for expected data checking.
- Customer Implementations

Customer Evaluation

Digital Blocks offers a variety of methods for prospective customers to evaluate the DB-I2C-S-SCL-CLK. Please contact Digital Blocks for additional information.

Deliverables

The DB-I2C-S-SCL-CLK is available in synthesizable RTL Verilog or a technology-specific netlist for FPGAs, along with Synopsys Design Constraints, a simulation test bench with expected results, datasheet, and user manual.

Ordering Information

Please contact Digital Blocks for additional technical, pricing, evaluation, and support information.

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