General Description

The Digital Blocks DB-SPI-FLASH-MEM-AXI is a Serial Peripheral Interface (SPI) Controller Verilog IP Core supporting access to Single/Dual/Quad SPI Flash Memory devices by way of Boot, Execute-in-Place (XIP), Processor Memory-Mapped IO, or optional DMA.

The DB-SPI-FLASH-MEM-AXI is a SPI Master Controller with two AMBA Slave Interfaces: One for Processor configuration or Processor access to the Flash Memory (i.e. Processor Memory-Mapped IO); the other, Slave AMBA Interface for Boot or Execute-in-Place (XIP) access to Flash Memory.

Figure 1 depicts the system view of the DB-SPI-FLASH-MEM Controller IP Core embedded within an integrated circuit device, with many optional Slave AMBA interface options. The specific DB-SPI-FLASH-AXI contains an AXI Slave allowing for Memory Read of Flash Memory via the SPI Master Bus, and AXI-Lite, AHB, or APB Slave Interface for Processor Configuration or Memory Read/Write of Flash Memory.

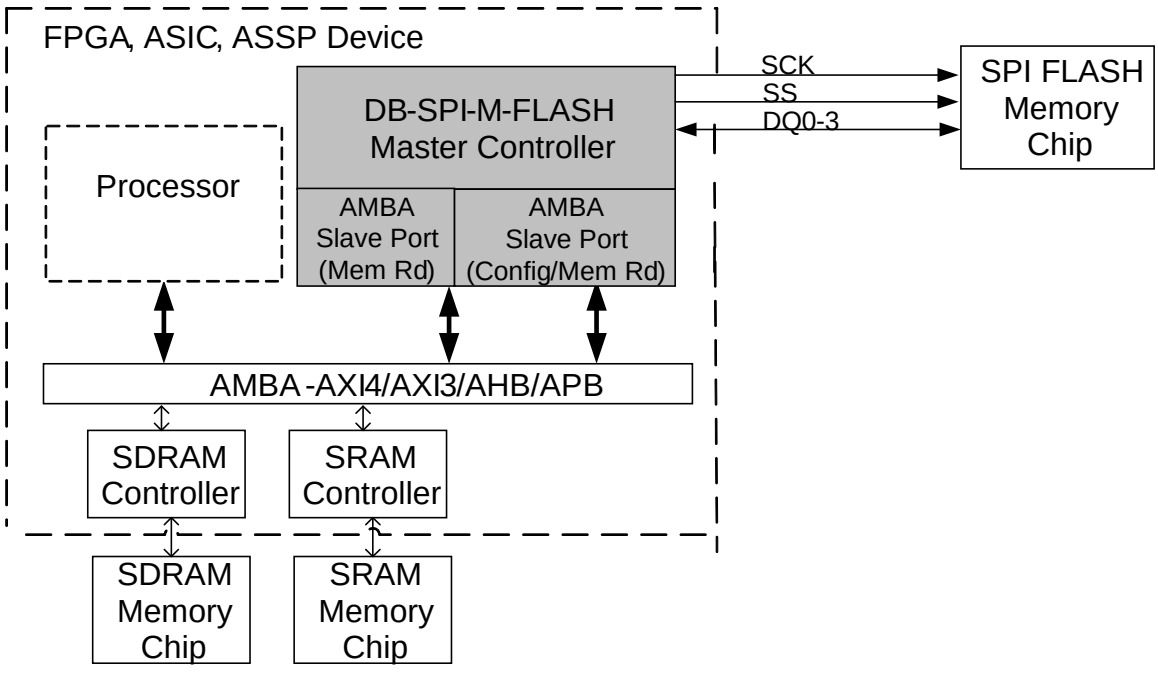

Figure 1: DB-SPI-FLASH-MEM-AXI Controller – System Diagram

Features

- Master SPI Controller with two interfaces to access SPI Flash Memory:
  - AXI Slave Interface for Execute-In-Place (XIP), boot – accepts AXI Slave read requests, reads the SPI Flash Memory, and returns the read data
  - APB Slave Interface for CPU direct read/write of SPI Flash Memory
- Signal Interface to SPI Flash Memory:
  - DQ/IO[3:0] - 1/2/4-bit Data
  - SCK - Serial Clock
  - SS[N:0] - Slave Select (i.e. Flash Memory)
- SPI Flash Memory:
  - Supports Boot, Execute-In-Place (XIP), CPU Programmable IO, or DMA
  - Flash Memory from Micron, Spansion, Winbond, Macronix
  - Supports SPI Mode0, Mode3 at 166 MHz
  - Up to N=8 Slave Select (SS) Outputs supporting multiple SPI Flash Memory devices
  - Configurable SPI Modes:
    - Standard SPI Mode (1 Data Lane)
    - Dual SPI Mode (2 Data lanes)
    - Quad SPI Mode (4 Data Lanes)
  - Programmable LSB-first or MSB-first Per Word
- Transmit/Receive FIFOs:
  - Dual-Clock designs
  - User configurable depths
- Two Clock Domains:
  - AMBA Bus / SCK Clocks
- Optional DMA Controller for transfers between System Memory & SPI Bus
- Internal interrupts with masking control
- Available AMBA Microprocessor Interfaces:
  - AXI / AHB / APB Buses
  - 8 / 16 / 32 bit Data Interface
- Compliance with ARM AXI4/ AXI3 / AHB / APB AMBA specifications:
  - Compliance with AMBA AXI Protocol Specification (V2.0)
  - Compliance with AMBA APB Protocol Specification (V3.0)
  - Compliance with AMBA Specification (V2.0) - AHB
  - Compliance with AMBA 3 AHB-Lite Protocol (V1.0)
- Compliance with ARM AMBA and Freescale / Motorola SPI specifications:
- Fully-synchronous, synthesizable Verilog RTL core, with rising-edge clocking, no gated clocks, and no internal tri-states, for easy integration into FPGA or ASIC design flows.

Pin Description

In addition to the two Slave AMBA Interfaces, which include the input CLOCK and RESET signals and the output INTR (interrupt) signal, the SPI interface signals are listed in Table 1.

Name	I/O	Description
SPI Bus Interface – Master – 4 Data lanes - Bidirectional		
DQ/IO[3:0]	I/O	**Data Input/Output–** SPI Master bidirectional serial data. SPI Flash Memory pins refer to these as DQ or IO.
SCKO	O	**Serial Clock Output** – Serial clock output
SSO[N:0]	O	**Slave Select Output** – Slave Select output. N can be up to 8 for multiple Flash Memory devices

Table 1: DB-SPI-FLASH-MEM – I/O Pin Description

Verification Method

The DB-SPI-M Controller IP Core contains a test suite with AMBA AXI, AHB, APB Bus functional models that program the DB-SPI-FLASH-MEM control & status registers, generates & sends SPI data, tests for Boot & XIP, monitors the SPI bus protocol, and checks expected results.

The DB-SPI-FLASH-MEM Controller IP Core have been Instantiated within a FPGA and ASICs (by customers) and verified with Micron, Spansion, Winbond, and Macronix Flash Memories.

Customer Evaluation

Digital Blocks offers a variety of methods for prospective customers to evaluate the DB-SPI-FLASH-MEM. Please contact Digital Blocks for additional information.

Deliverables

The SPI-FLASH-MEM is available in synthesizable RTL Verilog or a technology-specific netlist for FPGAs, along with Synopsys Design Constraints, a simulation test bench with expected results, datasheet, and user manual.

Ordering Information

Please contact Digital Blocks for additional technical, pricing, evaluation, and support information.

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