General Description

The Digital Blocks DB-AXI4-MM-TO-AXI4-STREAM-BRIDGE Verilog RTL IP Core accepts AXI4 Memory Map address, control, and data input, converts the address to an AXI4-Stream TID, and sends the data with TID out on the AXI4-Stream Interface.

The Digital Blocks DB-AXI4-MM-TO-AXI4-STREAM-BRIDGE IP Core works with Digital Blocks DMA Controller (i.e. the DB-DMAC-MC-AXI Verilog RTL IP Core) to transfer data from either memory or a peripheral to an AXI4-Stream peripheral or AXI4-Stream Network Interface.

Digital Blocks companion IP, the DB-AXI4-STREAM-TO-AXI4-MM-BRIDGE, works with Digital Blocks DMA Controller to transfers data from an AXI4-Stream peripheral or AXI4-Stream Network Interface to memory or another peripheral.

Figure 1 depicts DB-AXI4-MM-TO-AXI4-STREAM-BRIDGE Verilog IP Core.

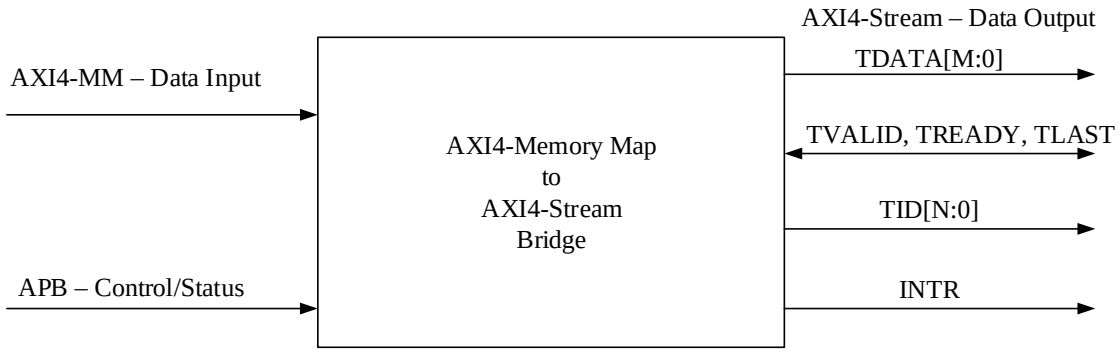

Figure 1: DB-AXI4-MM-TO-AXI4- STREAM-BRIDGE – Top Level View

Features

- Converts AXI4/AXI3 Memory Map Data & Control Interface into AXI4-Stream Interface
    - Standard release supports 16 AXI4-Stream Channels.
    - More or less Channels optional. Contact Digital Blocks with requirements.
- Works with Digital Blocks DMA Controller to support following data transfers:
    - Memory-to-Peripheral
    - Memory-to-Network
    - Peripheral-to-Peripheral
- Individual Interface Data Widths: 8 / 16 / 32 / 64 / 128 / 256 / 512 / 1024.
- Interrupt Controller – for Diagnostics
- Fully-synchronous, synthesizable Verilog RTL core, with rising-edge clocking, no gated clocks, and no internal tri-states, for easy integration into FPGA or ASIC design flows.

Verification Method

The DB-AXI4-MM-TO-AXI4-STREAM-BRIDGE IP Core contains a test suite that programs the IP and sources and receives data with checking results.

The DB-AXI4-MM-TO-AXI4-STREAM-BRIDGE Controller IP Core has been implemented in customer unique applications.

Customer Evaluation

Digital Blocks offers a variety of methods for prospective customers to evaluate the DB-AXI4-MM-TO-AXI4-STREAM-BRIDGE Controller IP Core. Please contact Digital Blocks for additional information.

Deliverables

The DB-AXI4-MM-TO-AXI4-STREAM-BRIDGE is available in synthesizable RTL Verilog or a technology-specific netlist for FPGAs, along with Synopsys Design Constraints, a simulation test bench with expected results, datasheet, and user manual.

Ordering Information

Please contact Digital Blocks for additional technical, pricing, evaluation, and support information.

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