

General Description

The Digital Blocks DB-DMAC-MC-AHB5 Verilog RTL IP Core is a Multi-Channel DMA Controller supporting 1 – 16 independent data transfers. The Direct Memory Access (DMA) Controller IP Core contains 1 - 16 DMA Controller Engines (i.e. DMA Channels), with a unified AHB5 Master Read/Write interconnects. The DB-DMAC-MC-AHB5 excels at high data throughput on both small and large data sets. Standard IP releases of number of DMA Controller Engines are 1, 2, 4, 8, and 16.

Figure 1 depicts the DMA Controller IP Core. The individual internal DMA Controller Engines are geared to perform high-bandwidth data transfers among memory and peripherals via the AHB5 interconnects.

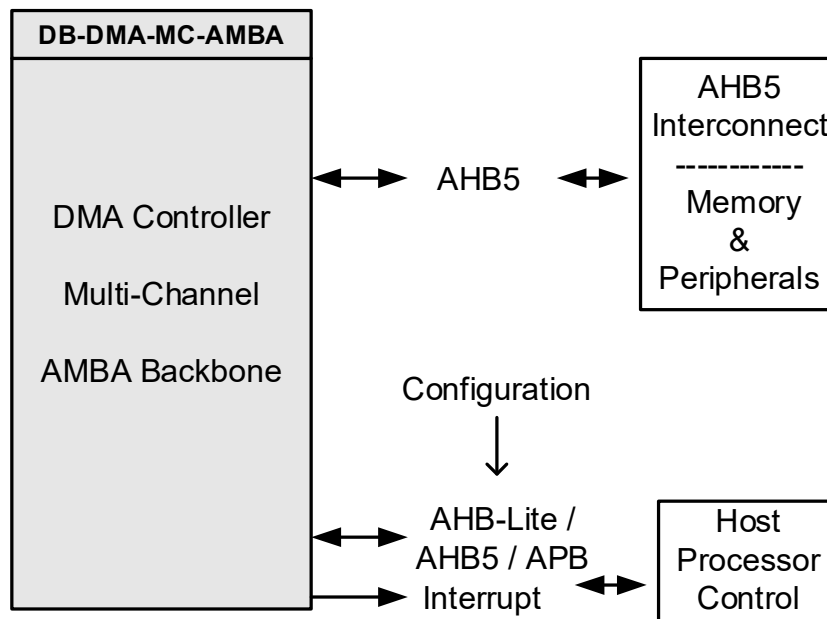


Figure 1: DB-DMA-MC-AHB5 – DMA Controller - Multi-Channel

Features

- 1 - 16 Multi-Channel High Performance DMA Controller Engines:
 - High-Speed Finite State Machine Control
 - High Throughput to/from Memory via AMBA AHB5 on both small and large data sets
 - Dual-Port, Single-Clock FIFO, user parameterized in Depth x Width.
 - Optional Dual-Port, Dual-Clock FIFO design
- Supports following DMA transfers:
 - Memory-to-Memory
 - Memory-to-Peripheral
 - Peripheral-to-Memory
 - Peripheral-to-Peripheral
- Up to 16 DMA transfers in parallel
- Scatter Gather List (SGL):
 - processing of linked-list Descriptor nodes
 - supports non-contiguous data block transfers to a contiguous segment of memory and vice versa
- Variety of User DMA Transfer Control:
 - Link-List Processor for Autonomous & Chained Block Transfers (SGL)
 - CPU Software or external Hardware initiated transfers
- Targets PCIe or CPU DMA Controller in Linux environment
- Arbiter – Round Robin (priority Arbitration Modes available – contact Digital Blocks)
- Individual Interface Data Widths: 8 / 16 / 32 / 64 / 128 / 256 / 512 / 1024.
- Programmable Data Burst Capability: 1, 4, 8, 16 and up to 256 via AHB5
- Interrupt Controller – Signaling DMA Status - Transfer Done & Diagnostics
- Fully-synchronous, synthesizable Verilog RTL core, with rising-edge clocking, no gated clocks, and no internal tri-states, for easy integration into FPGA or ASIC design flows.

Verification Method

The DB-DMAC-MC-AHB5 DMA Controller IP Core contains a test suite that programs the Controller and sources and receives with checking data transfers.

The DB-DMAC-MC-AHB5 DMA Controller IP Core has been implemented in a variety of Digital Blocks IP, including the 2D Graphics Hardware Accelerator, and Low Latency / High-Speed Networking RTP/TCP/UDP/IP Protocol Stack Processor.

The DB-DMAC-MC-AHB5 DMA Controller IP Core has been implemented in customer unique applications.

Customer Evaluation

Digital Blocks offers a variety of methods for prospective customers to evaluate the DB-DMAC-MC-AHB5 DMA Controller IP Core. Please contact Digital Blocks for additional information.

Deliverables

The DB-DMAC-MC-AHB5 is available in synthesizable RTL Verilog or a technology-specific netlist for FPGAs, along with Synopsys Design Constraints, a simulation test bench with expected results, datasheet, and user manual.

Ordering Information

Please contact Digital Blocks for additional technical, pricing, evaluation, and support information.

Digital Blocks, Inc.
PO Box 192
587 Rock Rd
Glen Rock, NJ 07452 USA
Phone: +1-201-251-1281
eFax: +1-702-552-1905
info@digitalblocks.com

Copyright © Digital Blocks, Inc. 2007 - 2022, ALL RIGHTS RESERVED

###

Digital Blocks is a registered trademark of Digital Blocks, Inc.
All other trademarks are the property of their respective owners