General Description

The Digital Blocks DB-DMAC-MC-AMBA SystemVerilog RTL IP Core is a Scatter-Gather (SG) Direct Memory Access (DMA) Controller with Master AXI4 Interconnect containing a parametrized configurable number of DMA Mult-Channels. Alternatively, there are DB-DMAC-MC-AMBA releases with fixed 2, 4, 8, and 16 DMA Channels offered at lower licensing cost. The DB-DMAC-MC-AMBA excels at high data throughput at low latency on both small and large data sets. Also available are AMBA AXI5 / AXI3 / AHB5 Master Read/Write interconnects.

Figure 1 depicts the DMA Controller IP Core. The individual internal DMA Controller Engines are geared to perform high-bandwidth data transfers with low latency among memory and peripherals via the AMBA interconnects.

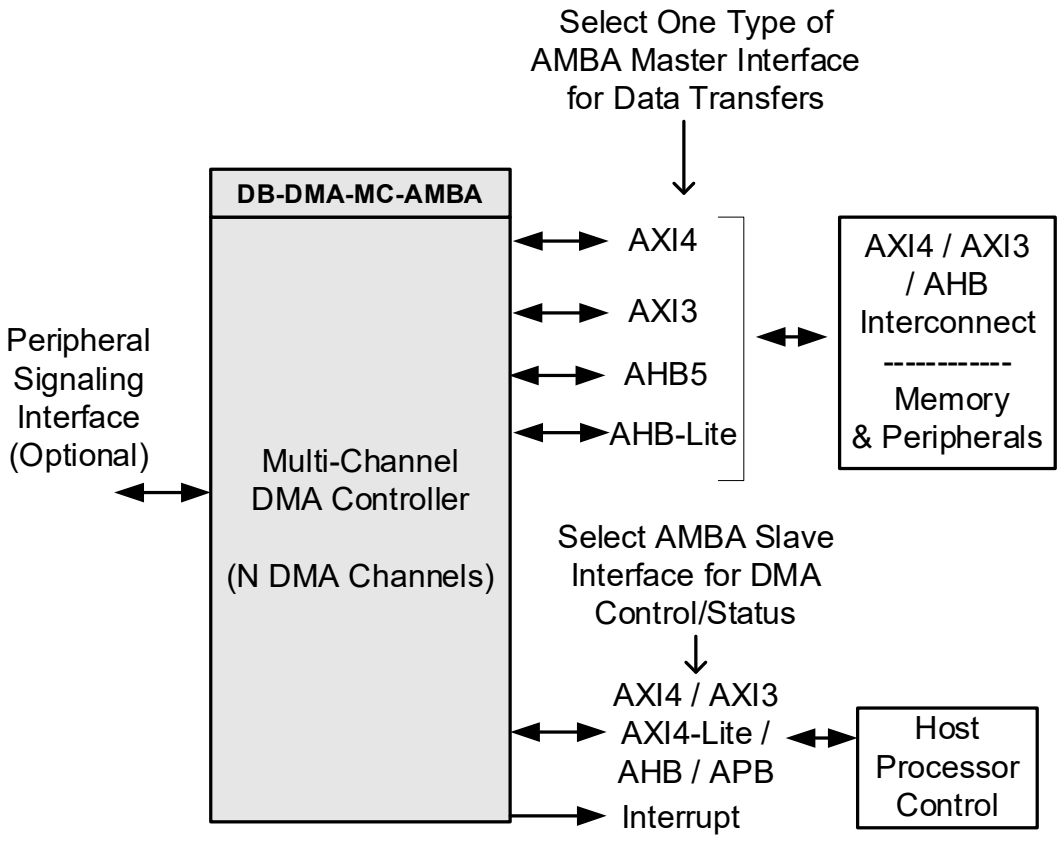

Figure 1: DB-DMA-MC-AMBA – DMA Controller - Multi-Channel

Features

- Parameter configurable number of DMA Channels
- Lower cost releases, containing fixed number DMA Channels of 2, 4, 8, or 16
- High Performance DMA Controller Engines:
  - High-Speed Finite State Machine Control
  - Up to 16 DMA transfers operational in parallel
  - High Throughput to/from Memory via AMBA AXI on both small and large data sets
  - Dual-Port, Single-Clock FIFO, user parameterized in Depth x Width.
  - Optional Dual-Port, Dual-Clock FIFO design
  - Optional external single memory interface for all DMA Multi-Channels
- Supports following DMA transfers:
  - Memory-to-Memory
  - Memory-to-Peripheral
  - Peripheral-to-Memory
  - Peripheral-to-Peripheral
- Scatter Gather List (SGL):
  - processing of linked-list Descriptor nodes
  - supports non-contiguous data block transfers to a contiguous segment of memory and vice versa
- Variety of User DMA Transfer Control:
  - Link-List Processor for Autonomous & Chained Block Transfers (SGL)
  - CPU Software or external Hardware initiated transfers
- Targets CPU DMA & PCIe DMA Controller in Linux environment as well as applications with standard peripherals or unique peripheral data transfer requirements
- Arbiter – Round Robin (priority Arbitration Modes available – contact Digital Blocks)
- Individual Interface Data Widths: 8 / 16 / 32 / 64 / 128 / 256 / 512 / 1024.
- Programmable Data Burst Capability: 1, 4, 8, 16 on AXI3/AHB5 and up to 256 on AXI4
- AXI4 Quality of Service (QoS) programming per DMA Channel (Option)
- AXI4-Stream to AXI Memory Map Conversion – external Digital Blocks IP to connect-in AXI4-Stream Interface (Please Contact Digital Blocks for more information) (Option)
- Interrupt Controller – Signaling DMA Status - Transfer Done & Diagnostics

- Fully-synchronous, synthesizable Verilog RTL core, with rising-edge clocking, no gated clocks, and no internal tri-states, for easy integration into FPGA or ASIC design flows.

Verification Method

The DB-DMAC-MC-AMBA DMA Controller IP Core contains a test suite that programs the Controller and sources and receives with checking data transfers.

The DB-DMAC-MC-AMBA DMA Controller IP Core has been implemented in a variety of customer applications.

Customer Evaluation

Digital Blocks offers a variety of methods for prospective customers to evaluate the DB-DMAC-MC-AMBA DMA Controller IP Core. Please contact Digital Blocks for additional information.

Deliverables

The DB-DMAC-MC-AMBA is available in synthesizable RTL Verilog or a technology-specific netlist for FPGAs, along with Synopsys Design Constraints, a simulation test bench with expected results, datasheet, and user manual.

Ordering Information

Please contact Digital Blocks for additional technical, pricing, evaluation, and support information.

Digital Blocks, Inc.
PO Box 192
587 Rock Rd
Glen Rock, NJ 07452 USA
Phone: +1-201-251-1281
eFax: +1-702-552-1905
info@digitalblocks.com