General Description

The Digital Blocks DB-DMAC-MC-AXI4-MM-STREAM Verilog RTL IP Core is a Multi-Channel Scatter-Gather DMA Controller that transfers data between AXI4 Memory Map and AXI4-Stream Interfaces.

Figure 1 depicts DB-DMAC-MC-AXI4-MM-STREAM Verilog IP Core.

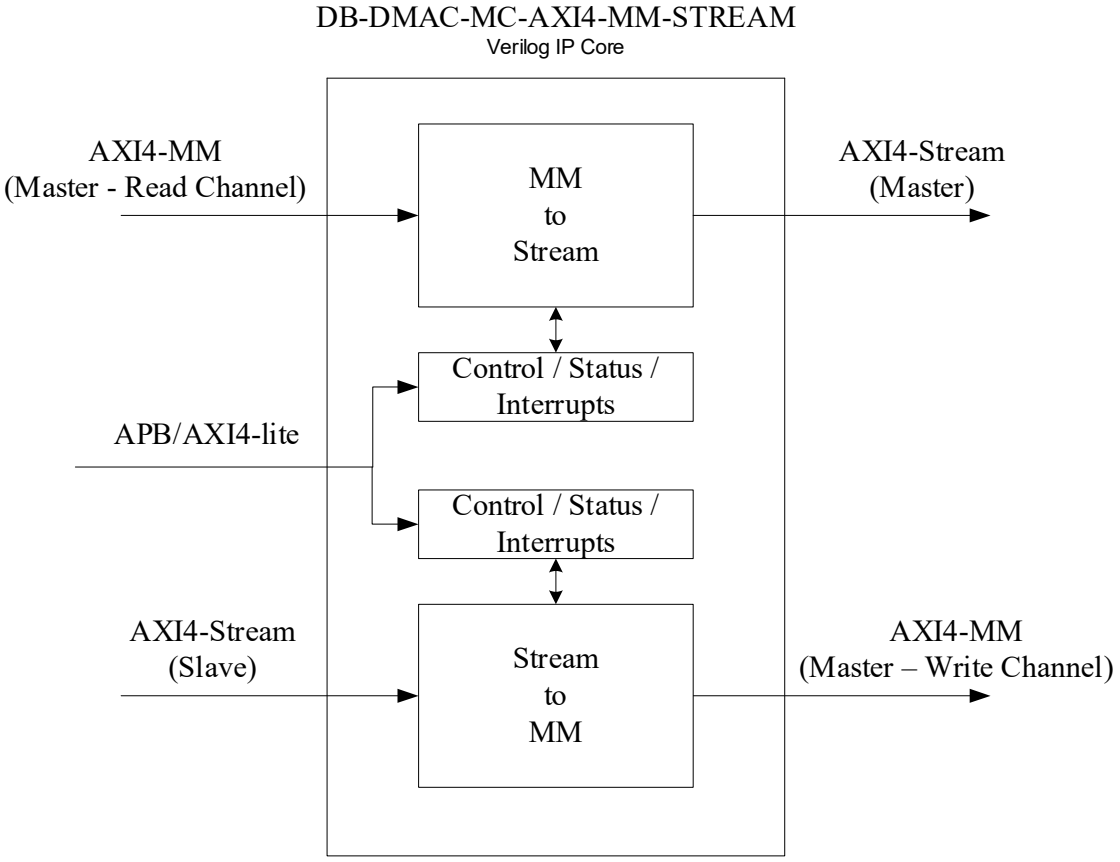

Figure 1: DB-DMAC-MC-AXI4-MM-STREAM – Top Level View

Features

- 2 Dedicated DMA Channels, 1 each for data transfers for the following:
  - Host Memory to Peripheral (AXI4-Memory Map to AXI4-Stream)
  - Peripheral to Host Memory (AXI4-Stream to AXI4-Memory Map)
- DMA Channel Features:
  - Scatter-Gather Descriptor Processor Engine
    - Descriptor FIFO to queue descriptors
  - Read & Write DMA Controller Engines
    - Data FIFO
  - Unaligned data transfers with byte realignment & using byte strobes
  - Advanced algorithm mapping AXI4-Memory Map address to/from AXI4-Stream sideband TID, TDEST, TUSER
  - Control / Status Registers accessible via APB/AXI4-Lite Interfaces
  - Parameters for FIFO width and depth
- AXI4 Interfaces:
  - AXI4-Memory Map Read Channel
  - AXI4-Memory Map Write Channel
  - Two AXI4-Stream Interfaces
  - Programmable Data Bursts: 1, 4, 8, 16 (fixed) and 1 – 256 (AXI4)
  - 4 KB boundary crossing detection & resizing of AXI transaction
  - Arbiter allows 2 Descriptor Engines and DMA Data Read to share single AXI4-Memory Map Read Channel to Host Memory
  - AXI4 Data Widths: 8 / 16 / 32 / 64 / 128 / 256 / 512 / 1024
- Interrupt Controller
- Configurations with more DMA Channels and AXI4-Stream Interfaces sharing same AXI4-Memory Map Read/Write Channels

Verification Method

The DB-DMAC-MC-AXI4-MM-STREAM IP Core contains a test suite that programs the IP and sources and receives data with checking results.

The DB-DMAC-MC-AXI4-MM-STREAM Controller IP Core has been implemented in customer unique applications.

Customer Evaluation

Digital Blocks offers a variety of methods for prospective customers to evaluate the DB-DMAC-MC-AXI4-MM-STREAM Controller IP Core. Please contact Digital Blocks for additional information.

Deliverables

The DB-DMAC-MC-AXI4-MM-STREAM is available in synthesizable RTL Verilog or a technology-specific netlist for FPGAs, along with Synopsys Design Constraints, a simulation test bench with expected results, datasheet, and user manual.

Ordering Information

Please contact Digital Blocks for additional technical, pricing, evaluation, and support information.

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