General Description

The Digital Blocks DB-DMAC-MC2-DL-MM2S-S2MM Verilog RTL IP Core is a Multi-Channel Scatter-Gather DMA Controller that transfers data between AXI4 Memory Map and AXI4-Stream Interfaces.

Control is managed by Descriptors initialized by the Control/Status Register Interface, with the Descriptors read in from memory via the AXI4 MM Read Channel and processed with the DMA data transfer information.

Digital Blocks offers two version releases of the DB-DMAC-MC2-DL-MM2S-S2MM:

- High AXI bandwidth throughput version with internal control plane that keeps the data interfaces transferring data at the full AXI Interface capabilities.
- Nominal bandwidth throughput version requiring less control plane VLSI resources at a lower licensing cost

Figure 1 depicts DB-DMAC-MC2-DL-MM2S-S2MM Verilog IP Core.

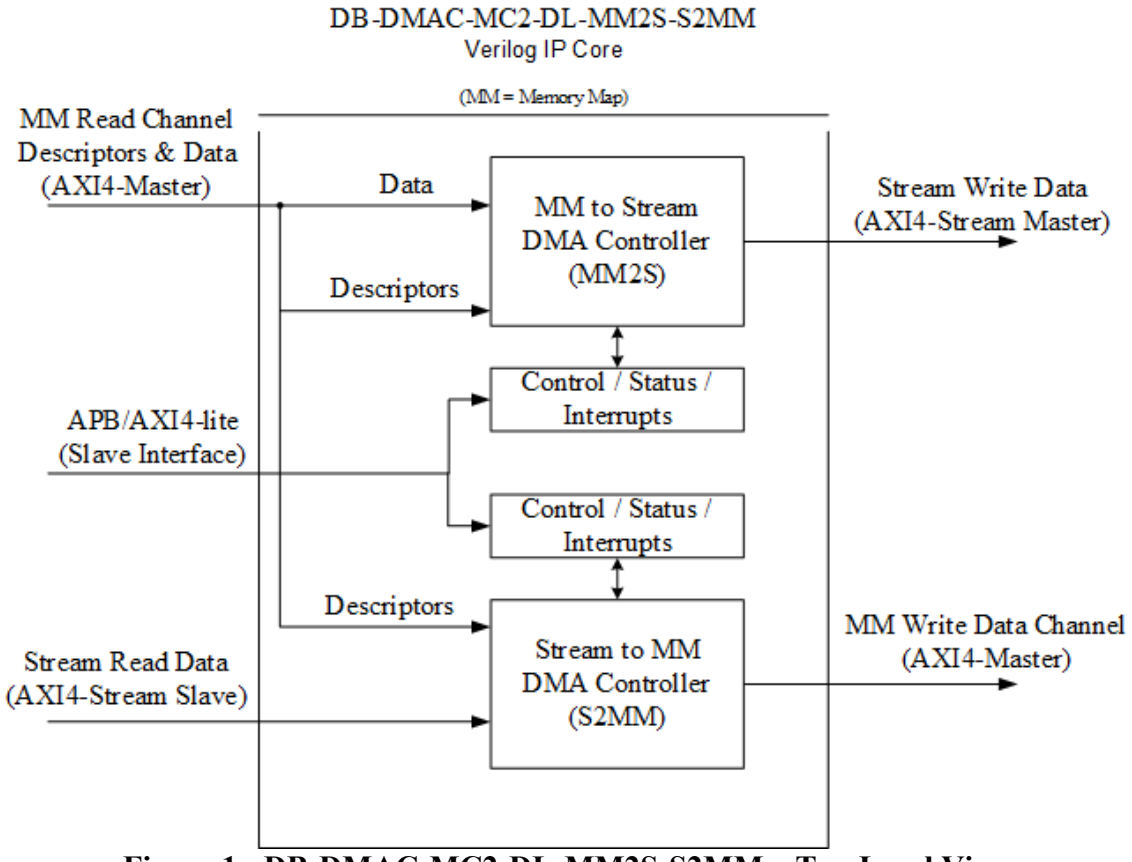

Figure 1: DB-DMAC-MC2-DL-MM2S-S2MM – Top Level View

Features

- 2 Dedicated DMA Channels, 1 each for data transfers for the following:
  - MM2S: AXI4-Memory Map Read Data to AXI4-Stream Write Data
  - S2MM: AXI4-Stream Read Data to AXI4-Memory Map Write Data
- Command and Status via Scatter Gather List (SGL) –
  - processing of linked-list Descriptor nodes
  - supports non-contiguous data block transfers to a contiguous segment of memory and vice versa
- Arbiter – Round Robin:
  - MM2S & S2MM request of the AXI4 Master Read Channel to read their Descriptors
  - MM2S request of the AXI4 Master Read Channel to read MM data
- MM2S & S2MM DMA Controllers:
  - Read & Write DMA Controller Engines
  - Data FIFO - Parameters for width and depth
  - Unaligned data transfers with byte realignment & using byte strobes
  - Releases versions supporting high or nominal AXI bandwidth throughput, with tradeoff in control plane VLSI resources and licensing cost
- Interrupt Controller – Signaling DMA Status - Transfer Done & Diagnostics
- Individual Interface Data Widths: 8 / 16 / 32 / 64 / 128 / 256 / 512 / 1024.
- Programmable Data Burst Capability: 1, 4, 8, 16 (fixed) and 1 – 256 (AXI4)
- 4 KB boundary crossing detection & resizing of AXI transaction
- Compliance with AMBA Specifications:
  - AXI4 Protocol Specification (Memory Map Read/Write Channels)
  - AXI4-Stream Protocol Specification
- Fully synchronous, synthesizable Verilog RTL core, with rising-edge clocking, no gated clocks, and no internal tri-states, for easy integration into FPGA or ASIC design flows.

Verification Method

The DB-DMAC-MC2-DL-MM2S-S2MM IP Core contains a test suite that programs the IP and sources and receives data with checking results.

The DB-DMAC-MC2-DL-MM2S-S2MM Controller IP Core has been implemented in customer unique applications.

Customer Evaluation

Digital Blocks offers a variety of methods for prospective customers to evaluate the DB-DMAC-MC2-DL-MM2S-S2MM Controller IP Core. Please contact Digital Blocks for additional information.

Deliverables

The DB-DMAC-MC2-DL-MM2S-S2MM is available in synthesizable RTL Verilog or a technology-specific netlist for FPGAs, along with Synopsys Design Constraints, a simulation test bench with expected results, datasheet, and user manual.

Ordering Information

Please contact Digital Blocks for additional technical, pricing, evaluation, and support information.

Digital Blocks, Inc.
PO Box 192
587 Rock Rd
Glen Rock, NJ 07452 USA
Phone: +1-201-251-1281
eFax: +1-702-552-1905
info@digitalblocks.com