

General Description

The Digital Blocks **DB-DMAC-MCn-AHB5** SystemVerilog RTL IP Core is a Scatter-Gather (SG) Direct Memory Access (DMA) Controller for AMBA 5 AHB systems, with a build-time number of independent DMA Channels (1 to 126) and a DMA data path of 8 to 1024 bits. It is the AHB5 member of the DB-DMAC-MC-AMBA family, next to the AXI4 and AXI5 controllers.

Each channel runs linked lists of 16-byte descriptor nodes with 32-bit addresses, any byte alignment and up to 16 MB per node, with read and write bursts of 4, 8 or 16 beats or a programmed length. A dedicated AHB5 Read Manager carries the descriptor fetches and source reads, and a dedicated AHB5 Write Manager the destination writes, so reads and writes run concurrently. Measured at 128 bits, two channels use **88.6 %** of the bus and one channel **79.6 %**.

1 - 126	8 - 1024	88.6 %	100 %
DMA channels, build-time option	bit DMA data path, 32-bit addressing	AHB5 bus use, 2 channels, 128-bit	branch / statement / FSM coverage, reviewed waivers

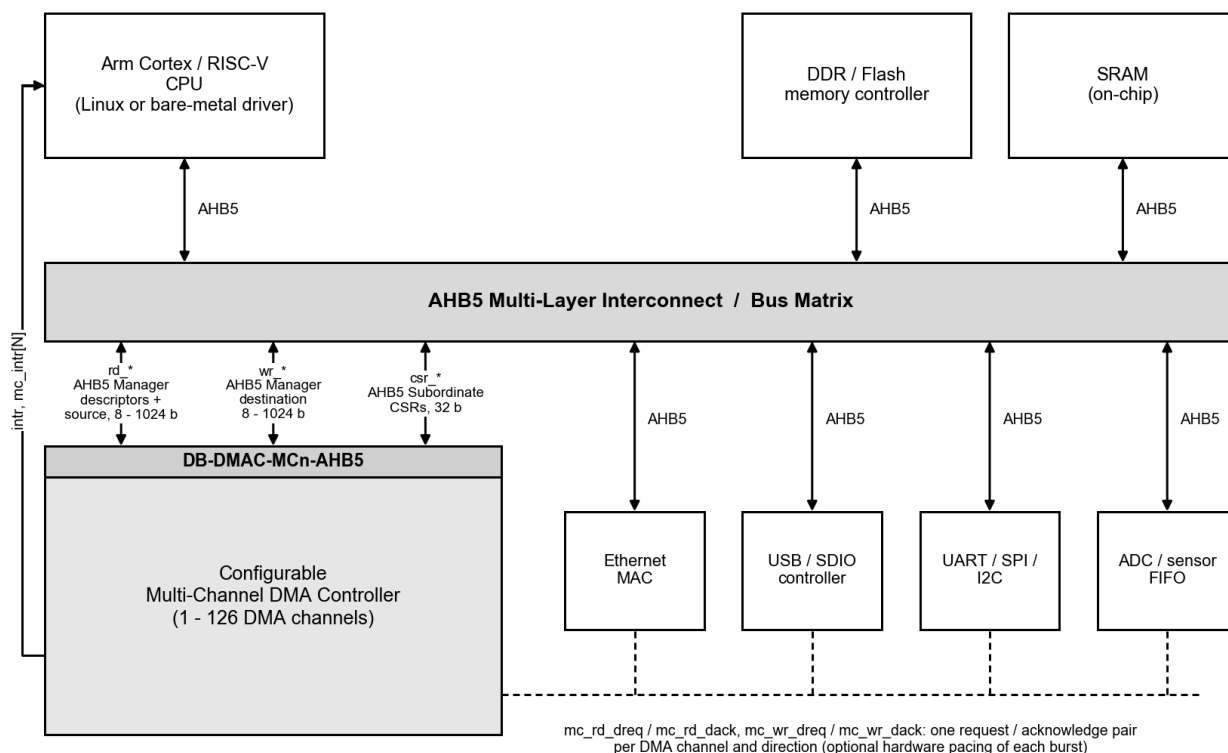


Figure 1: DB-DMAC-MCn-AHB5 in an SoC - memory-to-memory, memory-to-peripheral and peripheral-to-memory transfers over the AHB5 interconnect

Features

AHB5 Data Engine

- **Two AHB5 Managers:** a Read Manager for descriptor fetches and source data and a Write Manager for destination data, running concurrently
- **Programmable bursts:** INCR4, INCR8 or INCR16 per channel, or a programmed 1 to 256 beats (MCn-MB-AHB5) issued as INCR bursts of up to 16 beats; every burst is clipped at the 1 KB boundary and at the end of the block
- **Data FIFO:** 32 words of the data width per channel, with a byte rotator between the read and the write side
- Round-robin channel arbitration with an $O(\log N)$ parallel-prefix select on each AHB5 Manager; the grant is held for the whole burst; any number of wait states

Descriptor Processing

- Descriptor nodes are fetched over the Read Manager, one burst per 16-byte node (INCR4 at 32 bits, a single beat at 128 bits and wider)
- Per-channel pre-fetch of up to 32 descriptor nodes ahead of execution
- Descriptor list start / branch (DLB), re-start (DLR) and last-node address read-back (DLAR)

Scatter-Gather and Transfer Control

- Linked lists of 16-byte descriptor nodes: 32-bit source, destination and next address, 24-bit byte length (1 byte to 16 MB per descriptor node)
- Chained and ring descriptor structures with the descriptor node's NAV, LDN and WOR flags
- Memory-to-Memory, Memory-to-Peripheral, Peripheral-to-Memory, Peripheral-to-Peripheral
- Unaligned source and destination addresses at any byte, any length (byte rotator; naturally aligned narrow SINGLE transfers for the head and tail of the destination block); no burst crosses a 1 KB boundary
- Fixed-address (FIFO) reads and writes; hardware-paced bursts with per-channel DREQ / DACK pairs for reads and writes
- CPU software or external hardware initiated transfers

Status, Interrupts and Error Handling

- Per-channel status: descriptor list complete and channel done, descriptor read, source read and destination write ERROR responses, data and descriptor parity errors, re-start failure - each with an interrupt mask; a masked error holds the channel until cleared or reset
- Per-channel interrupt outputs; global interrupt status / mask / vector registers (one bank per 32 channels) and one processor interrupt
- Event-safe write-1-to-clear: a hardware event in the same cycle as the clear is never lost
- Optional per-byte parity checking on data and descriptor reads; parity generated on writes
- TrustZone: per-channel HNONSEC and HPROT for each Manager, and a security lock that hides a channel's registers from Non-secure accesses
- Core Identification Register (CIR): vendor, channel count, data width, bus, security and unaligned-addressing flags, revision

Integration

- 1 to 126 channels (one global interrupt bank per 32); data width 8 / 16 / 32 / 64 / 128 / 256 / 512 / 1024 bits; 32-bit addressing
- SystemVerilog RTL with a flat-pin top level; AMBA 5 AHB Manager / Subordinate naming
- Elaboration-time checks reject illegal configuration values
- Fully synchronous single clock, rising-edge, no gated clocks, no internal tri-states; technology-independent RTL for ASIC and FPGA
- Sister products for AXI systems: DB-DMAC-MCn-AXI4, DB-DMAC-MCn-AXI4-HT and DB-DMAC-MCn-AXI5-HT

Applications

- Memory-to-memory copy engines in AHB5 microcontroller and SoC subsystems
- Scatter-gather DMA for networking, storage and sensor data movement
- Peripheral data streaming with hardware request / acknowledge pacing
- Offload of bulk memory copies from the CPU, under Linux or bare metal

Architecture

Figure 2 shows the internal structure. Each DMA channel has its own registers, descriptor processor, 32-descriptor-node pre-fetch FIFO, control unit, read and write engines and a 32-word data FIFO with a byte rotator. Two shared AHB5 Managers serve all channels: the Read Manager arbitrates every channel's descriptor fetches and data reads, the Write Manager its data writes, including the narrow head and tail transfers of unaligned blocks. The numbered tags mark the blocks in the table below.

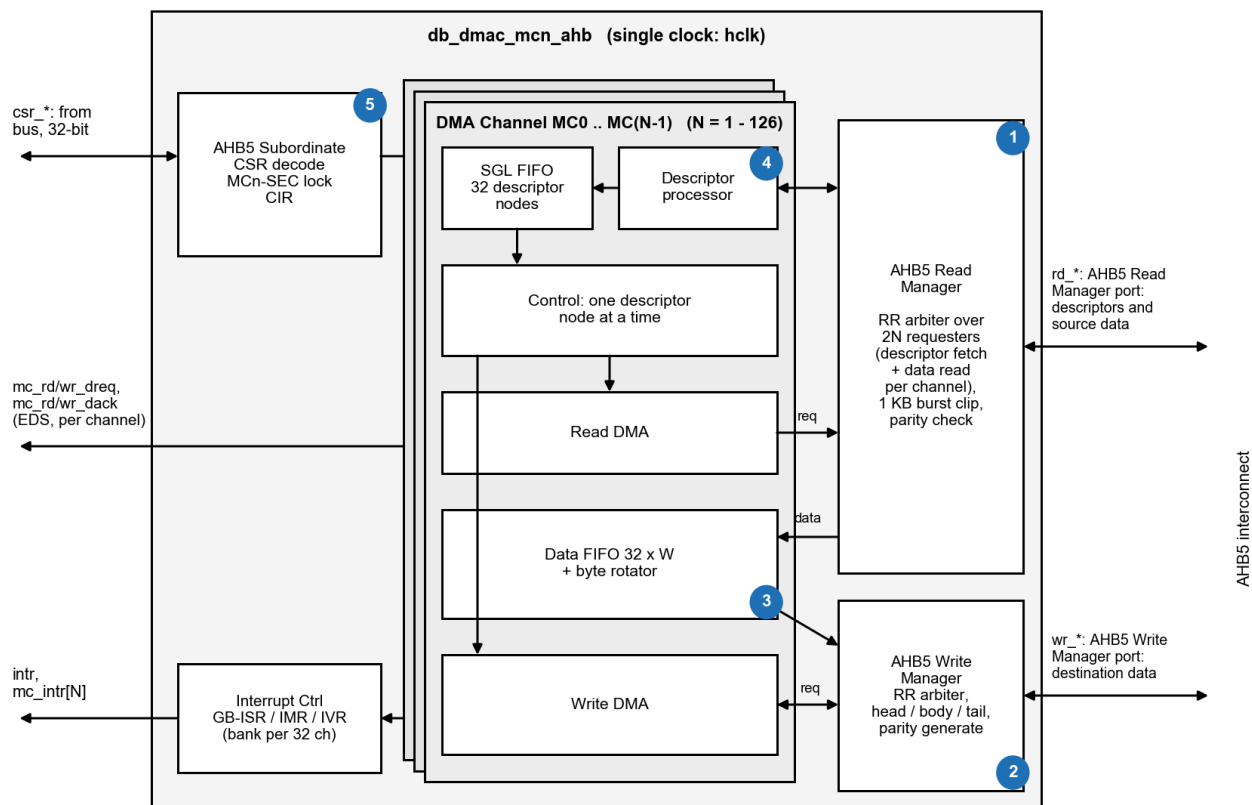


Figure 2: DB-DMAC-MCn-AHB5 internal architecture

#	Block	Function
1	AHB5 Read Manager	Descriptor fetches and source reads of every channel; SINGLE / INCR4 / 8 / 16 / INCR bursts
2	AHB5 Write Manager	Destination writes: full-width bursts plus narrow head / tail SINGLE transfers
3	Data FIFO + rotator	32 x W per channel; any source / destination byte offset
4	Descriptor processor	16-byte nodes, up to 32 pre-fetched; branch, re-start, ring (WOR)
5	Register port	32-bit AHB5 Subordinate, zero wait states; per-channel security lock (MCn-SEC)

Data flow: software writes the first descriptor node address and starts the channel. The descriptor processor fetches descriptor nodes over the Read Manager and queues them; the control unit loads the read and write engines; read bursts fill the data FIFO, the rotator shifts bytes for unequal source / destination offsets and the write engine drains the FIFO. A descriptor node completes when its last write beat has been accepted by the subordinate; the channel then raises its completion status and interrupt.

Measured Performance

Cycle-accurate RTL simulation of a 128-bit build (16 bytes per hclk cycle peak on each Manager) against AHB5 memory models with full-rate HREADY and programmable wait states, counted from the first descriptor fetch to the last accepted write beat.

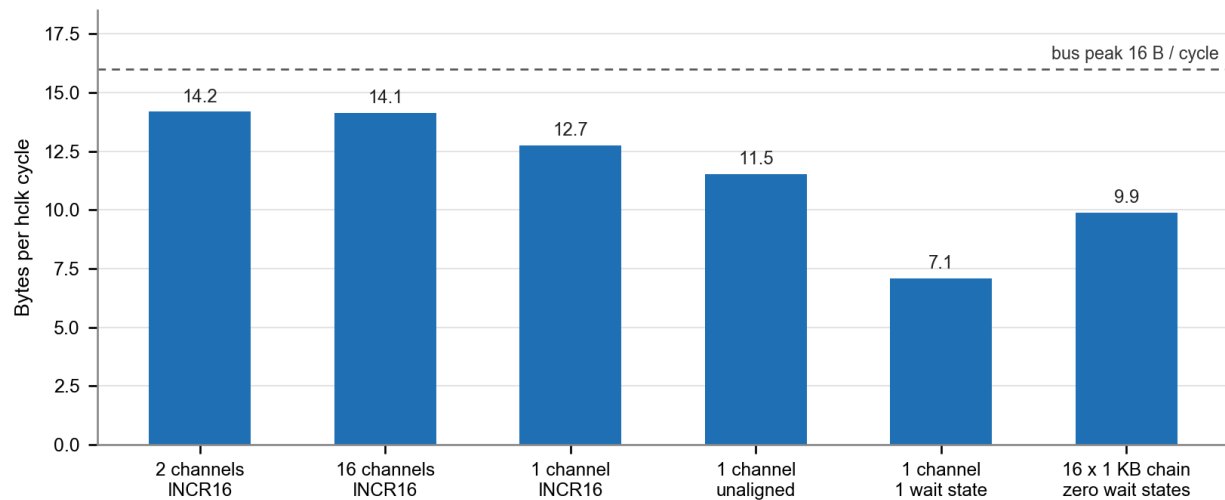


Figure 3: Measured throughput, 128-bit data path (bytes per hclk cycle)

Scenario	Conditions	Bytes / cycle	Bus use
Two channels in parallel, 64 KB each	INCR16 bursts, zero wait states	14.18	88.6 %
Sixteen channels in parallel, 8 KB each	INCR16 bursts, zero wait states	14.12	88.3 %
One channel, 64 KB copy	INCR16 bursts, zero wait states	12.73	79.6 %
One channel, 64 KB copy	INCR4 bursts, zero wait states	7.99	49.9 %
One channel, 64 KB copy, unaligned	Source offset 1, destination offset 3, INCR16 bursts, zero wait states	11.53	72.1 %
One channel, 64 KB copy	INCR16 bursts, 1 wait state on every read and write beat	7.08	44.2 %
Scatter-gather chain of 16 x 1 KB descriptor nodes	INCR16 bursts, zero wait states	9.88	61.8 %
Descriptor node boundary cost	16 x 1 KB descriptor nodes vs one 16 KB descriptor node, zero wait states	23 cycles per boundary	-

The 32-bit default build gives the same bus use: two channels 3.55 B / cycle (88.8 %), one channel 3.20 B / cycle (79.9 %). One channel takes about 20 cycles per 16-beat burst (INCR8: 66.5 %, INCR4: 49.9 %); a second channel fills the gaps. With one wait state on every beat the ceiling is 50 %. Figures scale with the data width; results depend on the interconnect, memory and configuration. Measured on the Rel_1_2_33 RTL.

Interfaces

AMBA terminology used in this data sheet: an AHB5 Manager issues transfers (formerly 'AHB Master'); an AHB5 Subordinate responds to them (formerly 'AHB Slave'). The ports are grouped by signal prefix as follows:

Interface	Type	Width	Function
rd_*	AHB5 Manager (read)	Data 8 - 1024 Address 32	Descriptor node fetches and DMA source reads. SINGLE, INCR4 / 8 / 16 and INCR bursts, never across 1 KB; HPROT[6:0] and HNONSEC per channel; per-byte read-data parity (optional)
wr_*	AHB5 Manager (write)	Data 8 - 1024 Address 32	DMA destination writes: full-width bursts plus naturally aligned narrow SINGLE transfers at unaligned heads and tails; HPROT[6:0] and HNONSEC per channel; per-byte write-data parity
csr_*	AHB5 Subordinate	Data 32 Address 32	Control / status registers, 4 KB window, 32-bit word access, zero wait states, OKAY response; unused offsets read 0; HNONSEC-aware channel lock
mc_rd_dreq / dack mc_wr_dreq / dack	Request / acknowledge	1 per channel	Hardware pacing of individual read and write bursts by a peripheral (EDS-R / EDS-W)
intr, mc_intr[N]	Level interrupt	1 + N	Processor interrupt and per-channel interrupts
hclk, hresetn	Clock / reset	1, 1	Single clock; active-low asynchronous reset
scan_mode	DFT	1	Holds the per-channel software reset inactive during scan

Verification

The DB-DMAC-MCn-AHB5 is delivered with the self-checking test bench used for sign-off. It programs the controller, sources and checks every transferred byte, and runs channel- and width-generic scenarios over every configured channel. AHB5 memory models inject wait states, ERROR responses and parity errors; AHB5 protocol assertions on both Managers and the register port and a descriptor-length monitor run in every test. Rel_1_2_33 sign-off: 35 / 35 tests in the default build (16 channels, 32 bits), all generic tests in 13 channel-count and data-width builds (1 to 126 channels, 8 to 1024 bits), and 100 % branch, statement and FSM coverage after reviewed waivers (99.76 % before).

Deliverables

Item	Contents
RTL	Synthesizable SystemVerilog (IEEE 1800-2012) with a flat-pin top level; or a technology-specific netlist for FPGAs
Constraints / filelists	Synopsys Design Constraints, compile-ordered filelist, lint script and waivers
Test bench	Self-checking directed and generic suites, AHB5 memory models, AHB5 protocol assertions, regression driver with expected results and coverage scripts
Models	C++ cycle model build
Software	Bare-metal C driver with reference program; Linux platform driver, UAPI header and device-tree example
Documents	Data sheet, Technical Reference Manual, IP Integration Guide, IP-XACT component descriptor, coverage report, test matrix, regression evidence

Ordering Information

Digital Blocks offers a variety of methods for prospective customers to evaluate the DB-DMAC-MCn-AHB5. Please contact Digital Blocks for additional technical, pricing, evaluation and support information. DMA

controllers for AXI4 (DB-DMAC-MCn-AXI4) and high-throughput variants for AXI4 (DB-DMAC-MCn-AXI4-HT) and AXI5 (DB-DMAC-MCn-AXI5-HT) are also available.

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