Digital Blocks

Semiconductor IP

DB-DMAC-MCn-AXI4

Configurable Multi-Channel DMA Controller

Scatter-Gather | AMBA AXI4 | 1 - 126 Channels

General Description

The Digital Blocks **DB-DMAC-MCn-AXI4** SystemVerilog RTL IP Core is a Scatter-Gather (SG) Direct Memory Access (DMA) Controller for AMBA AXI4 systems, with a build-time number of independent DMA Channels (1 to 126) and a DMA data path of 64 to 512 bits. It is the configurable member of the DB-DMAC-MC-AMBA family: the register model, descriptor format and drivers of the high-throughput DB-DMAC-MCn-AXI4-HT, in the smallest implementation.

Each channel runs linked lists of descriptor nodes with 64-bit addresses, any byte alignment and up to 16 MB per node, with read and write bursts of 4, 8, 16 or a programmed 1 to 256 beats and up to 16 requests outstanding. One AXI4 Manager port carries the descriptor fetches and the DMA data of every channel. Measured at 128 bits, two channels use **86.7 %** of the bus and one channel with programmed 32-beat bursts **85.3 %**.

1 - 126	**64 - 512**	**86.7 %**	**99.9 %**
DMA channels, build-time option	bit DMA data path, 64-bit addressing	AXI4 bus use, 2 channels, 128-bit	branch / statement coverage, 100 % FSM coverage

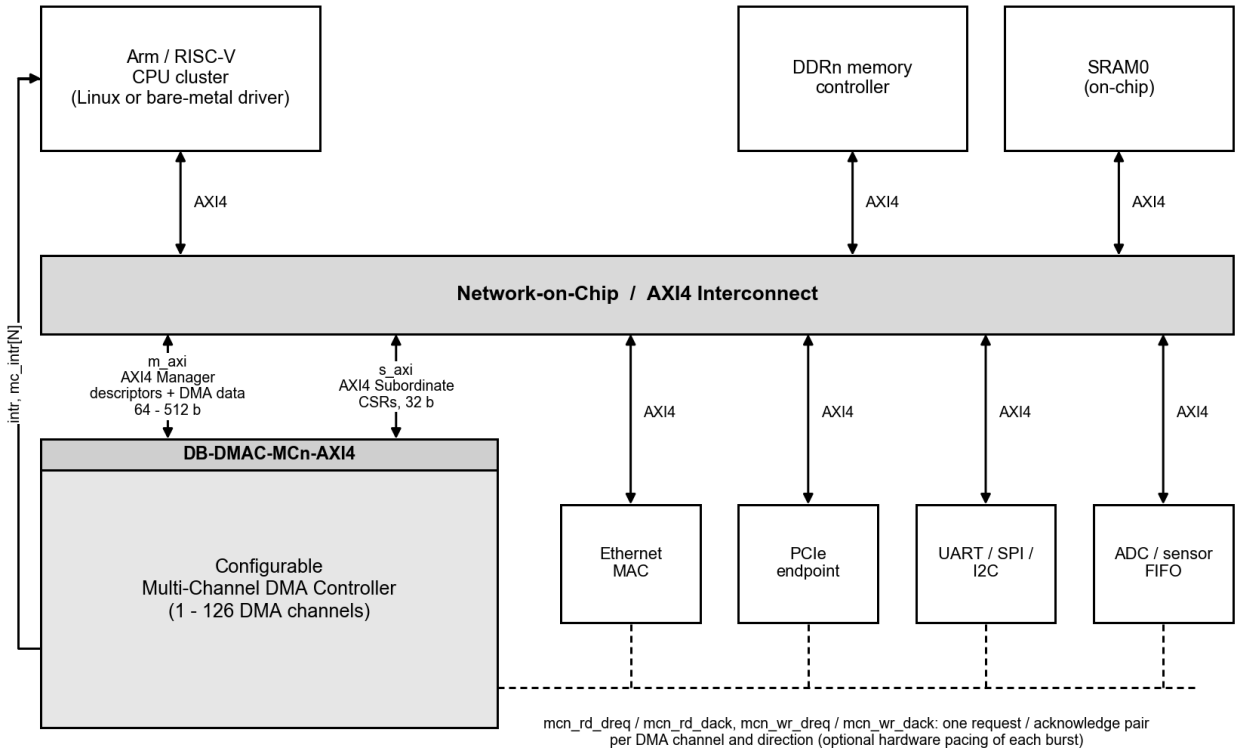


Figure 1: DB-DMAC-MCn-AXI4 in an SoC - memory-to-memory, memory-to-peripheral and peripheral-to-memory transfers over the NoC

Features

AXI4 Data Engine

- **Programmable bursts**: read and write bursts of 4, 8 or 16 beats, or a programmed 1 to 256 beats per channel (MCn-MB-AXI4); INCR or FIXED addressing
- **Outstanding requests**: 1, 2, 4, 8 or 16 reads and writes outstanding per channel, bounded by the per-channel data FIFO (see the TRM)
- **Data FIFO**: 256 words of the data width per channel, with a byte realigner between the read and the write side
- Round-robin channel arbitration with an O(log N) parallel-prefix select on each AXI4 Manager; per-channel ARQOS / AWQOS, descriptor fetches at ARQOS 0xF

Descriptor Processing

- Descriptor nodes are fetched over m_axi, one 256-bit read per node (4 beats at 64 bits, 1 beat at 256 bits)
- Per-channel pre-fetch of up to 32 descriptor nodes ahead of execution
- Descriptor list start / branch (DLB) and re-start (DLR) at any time

Scatter-Gather and Transfer Control

- Linked lists of 32-byte descriptor nodes: 64-bit source, destination and next address, 24-bit byte length (1 byte to 16 MB per descriptor node)
- Chained and ring descriptor structures with the descriptor node's NAV, LDN and WOR flags
- Memory-to-Memory, Memory-to-Peripheral, Peripheral-to-Memory, Peripheral-to-Peripheral
- Unaligned source and destination addresses at any byte, any length (byte rotator, WSTRB on the first and last word); automatic split at 4 KB boundaries
- Fixed-address (FIFO) reads and writes; hardware-paced bursts with per-channel DREQ / DACK pairs for reads and writes
- CPU software or external hardware initiated transfers

Status, Interrupts and Error Handling

- Per-channel status: descriptor list and descriptor node complete, descriptor read, source read and destination write errors, data and descriptor parity errors, re-start failure - each with an interrupt mask; a masked error holds the channel until cleared or reset
- Per-channel interrupt outputs; global interrupt status / mask / vector registers and one processor interrupt
- Event-safe write-1-to-clear: a hardware event in the same cycle as the clear is never lost
- Optional per-byte parity checking on data and descriptor reads; parity generated on writes
- Core Identification Register (CIR): vendor, channel count, address width, bus and revision

Integration

- 1 to 126 channels (one global interrupt bank per 32); data width 64 / 128 / 256 / 512 bits; 64-bit addressing
- SystemVerilog RTL with a flat-pin top level; AMBA AXI4 Manager / Subordinate naming
- Elaboration-time checks reject illegal configuration values
- Fully synchronous single clock, rising-edge, no gated clocks, no internal tri-states; technology-independent RTL for ASIC and FPGA
- Upgrade path: the DB-DMAC-MCn-AXI4-HT keeps the register model, descriptor format and drivers

Applications

- Memory-to-memory copy engines in SoCs
- Scatter-gather DMA for networking, storage and PCIe endpoint data movement
- Peripheral data streaming with hardware request / acknowledge pacing
- Offload of bulk memory copies from CPU clusters, under Linux or bare metal

Architecture

Figure 2 shows the internal structure. Each DMA channel has its own registers, descriptor processor, 32-descriptor-node pre-fetch FIFO, control unit, read and write engines and a 256-word data FIFO with a byte realigner. Two shared AXI4 Managers serve all channels on the m_axi port: the read manager arbitrates every channel's descriptor

fetches and data reads (AR / R), the write manager its data writes (AW / W / B). The numbered tags mark where the DB-DMAC-MCn-AXI4-HT differs (table below).

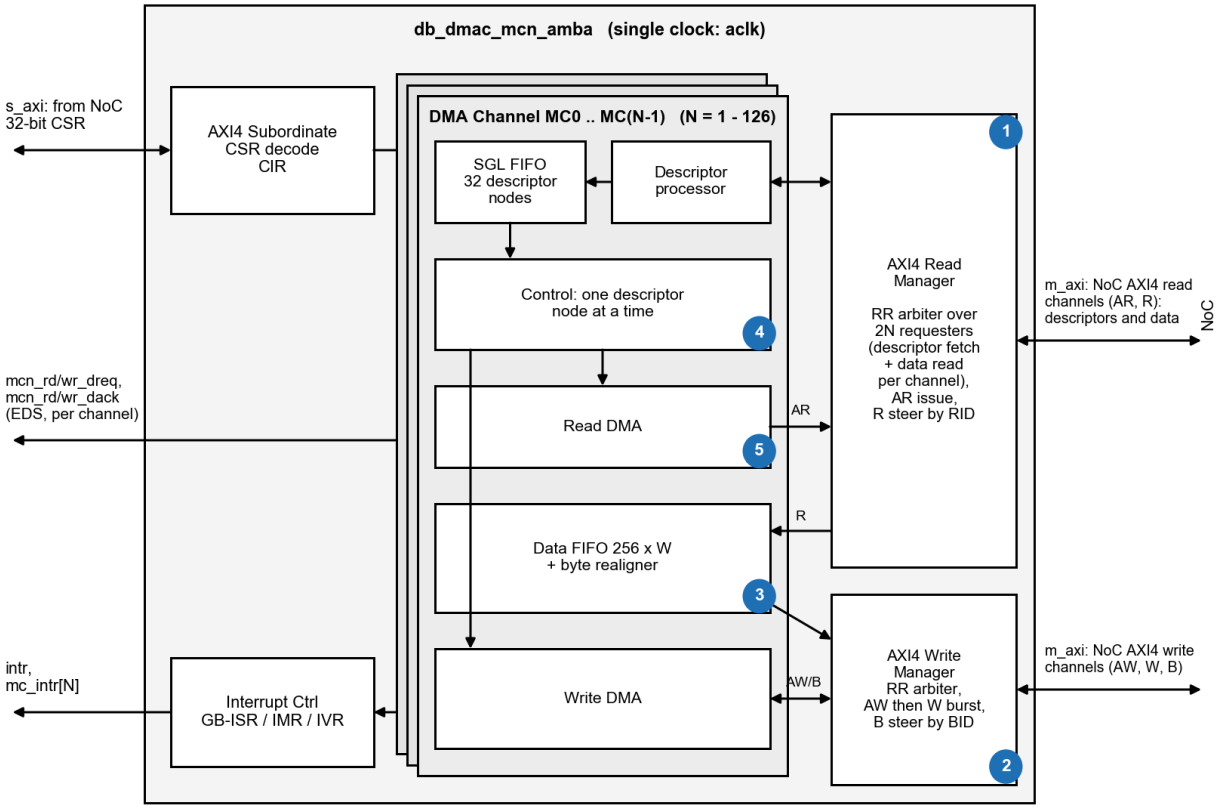


Figure 2: DB-DMAC-MCn-AXI4 internal architecture

#	Feature	DB-DMAC-MCn-AXI4 / DB-DMAC-MCn-AXI4-HT
1	Manager ports	One m_axi for descriptors and data / m_axi for data plus a dedicated d_axi for descriptors
2	Write path	Each W burst follows its AW handshake / AW queue, W bursts back-to-back
3	Read buffering	FIFO space checked per request / space reserved at issue, RREADY = 1
4	Descriptor node boundary	24 cycles / 2 cycles (descriptor overlap)
5	One channel, 200-cycle read latency	4.5 B / cycle / 11.7 B / cycle (128-bit)

Data flow: software writes the first descriptor node address and starts the channel. The descriptor processor fetches descriptor nodes over m_axi and queues them; the control unit loads the read and write engines; read bursts fill the data FIFO, the realigner rotates bytes for unequal source / destination offsets and the write engine drains the FIFO. A descriptor node completes when its last write response is in, so its data is committed; the channel then updates its last-descriptor-node address and raises its completion interrupt.

Measured Performance

Cycle-accurate RTL simulation of the default build (128-bit AXI4 Manager, 16 bytes per cycle peak) against an AXI4 memory model with full-rate READY and programmable read and write-response latency; each scenario uses its best tested channel setting.

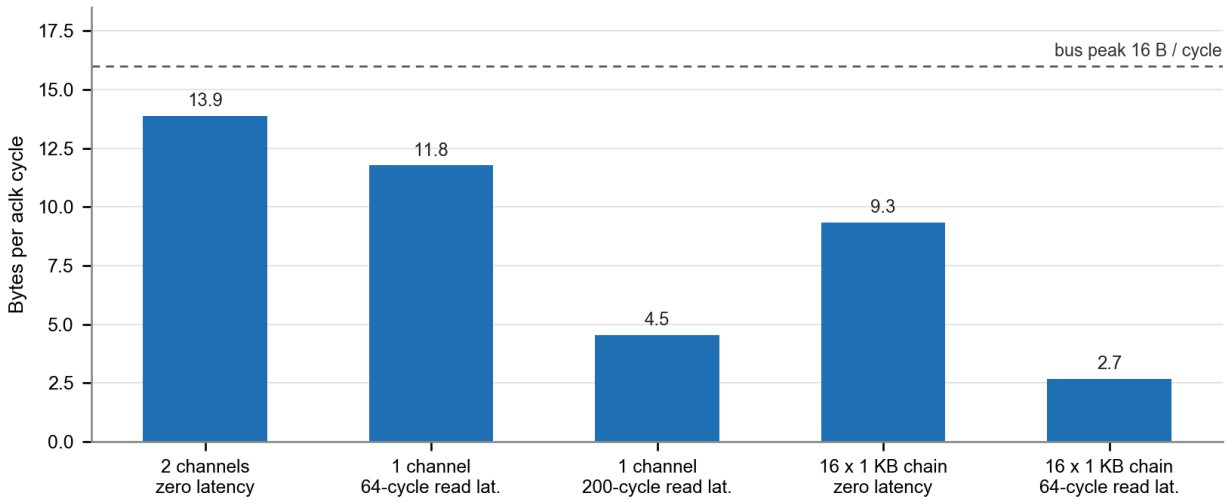


Figure 3: Measured throughput, 128-bit data path (bytes per aclk cycle)

Scenario	Conditions	Bytes / cycle	Bus use
Two channels in parallel, 64 KB each	16-beat bursts, zero memory latency	13.87	86.7 %
One channel, 64 KB copy	16-beat bursts, 4 reads outstanding, read latency 64, B latency 16	11.77	73.5 %
One channel, 64 KB copy	16-beat bursts, 4 reads outstanding, read latency 200, B latency 50	4.54	28.4 %
Scatter-gather chain of 16 x 1 KB descriptor nodes	16-beat bursts, zero memory latency	9.35	58.4 %
Scatter-gather chain of 16 x 1 KB descriptor nodes	read latency 64, B latency 16	2.68	16.7 %
Descriptor node boundary cost	16 x 1 KB descriptor nodes vs one 16 KB descriptor node, zero latency	24 cycles per boundary	-

One channel at zero latency reaches 13.65 B / cycle (85.3 %) with programmed 32-beat bursts. At 200-cycle read latency one channel sustains 4.5 B / cycle with 4 reads outstanding (1.2 B / cycle with one); the DB-DMAC-MCn-AXI4-HT sustains 11.7 B / cycle in the same test. Figures scale with the data width; results depend on the interconnect, memory and configuration. Measured with the DB-DMAC-MCn-AXI4-HT performance test bench on the Rel_1_2_54 data engine (unchanged in Rel_1_2_55).

Interfaces

AMBA terminology used in this data sheet: an **AXI4 Manager** issues transactions (formerly 'AXI4 Master'); an **AXI4 Subordinate** responds to them (formerly 'AXI4 Slave'). The five AXI4 channels are abbreviated as follows:

Interface	Type	Width	Function
m_axi	AXI4 Manager (AR, R, AW, W, B)	Data 64 - 512 Address 64	Descriptor node fetches and DMA data reads and writes. INCR / FIXED bursts up to 256 beats, two IDs per channel (descriptor, data), multiple outstanding transactions, read data interleaved across IDs, AxQOS, per-byte data parity
s_axi	AXI4 Subordinate	Data 32 Address 32	Control / status registers, 4 KB window, single-beat; SLVERR on reads of unused offsets. Connects to AXI4-Lite through a bridge or simple tie-offs
mcn_rd_dreq / dack mcn_wr_dreq / dack	Request / acknowledge	1 per channel	Hardware pacing of individual read and write bursts by a peripheral (EDS-R / EDS-W)
intr, mc_intr[N]	Level interrupt	1 + N	Processor interrupt and per-channel interrupts
aclk, aresetn	Clock / reset	1, 1	Single clock; active-low asynchronous reset
scan_mode	DFT	1	Holds the per-channel software reset inactive during scan

Verification

The DB-DMAC-MCn-AXI4 is delivered with the self-checking test bench used for sign-off. It programs the controller, sources and checks every transferred byte, and runs channel- and width-generic scenarios over every configured channel. Memory models inject wait states on every channel, read interleaving across IDs, SLVERR responses and parity errors; FIFO assertions run in every test. Rel_1_2_55 sign-off: 36 / 36 tests in the default build, all tests in 14 channel-count and data-width builds (1 to 126 channels, 64 to 512 bits), and 99.88 % branch, 99.92 % statement and 100 % FSM coverage.

Deliverables

Item	Contents
RTL	Synthesizable SystemVerilog (IEEE 1800-2012) with a flat-pin top level; or a technology-specific netlist for FPGAs
Constraints / filelists	Synopsys Design Constraints, compile-ordered filelist, lint script and waivers
Test bench	Self-checking directed and generic suites, AXI4 memory models, FIFO assertions, regression driver with expected results and coverage scripts
Models	C++ cycle model build
Software	Bare-metal C driver with reference program; Linux platform driver, UAPI header and device-tree example
Documents	Data sheet, Technical Reference Manual, IP Integration Guide, coverage report, test matrix, regression evidence

Ordering Information

Digital Blocks offers a variety of methods for prospective customers to evaluate the DB-DMAC-MCn-AXI4. Please contact Digital Blocks for additional technical, pricing, evaluation and support information. Fixed-channel

versions (2, 4, 8 or 16 channels) are available at a lower license cost; high-throughput variants for AXI4 (DB-DMAC-MCn-AXI4-HT) and AXI5 (DB-DMAC-MCn-AXI5-HT) are also available.

Digital Blocks, Inc.
PO Box 192
587 Rock Rd
Glen Rock, NJ 07452 USA
Phone: +1-551-258-0412
info@digitalblocks.com

Copyright © Digital Blocks, Inc. 2007 - 2026, ALL RIGHTS RESERVED
Digital Blocks is a registered trademark of Digital Blocks, Inc. AMBA and Arm are registered trademarks of Arm Limited. All other trademarks are the property of their respective owners.