Digital Blocks

Semiconductor IP

DB-DMAC-MCn-AXI4-HT

High-Throughput Multi-Channel DMA Controller

Scatter-Gather | AMBA AXI4 | 1 - 126 Channels

General Description

The Digital Blocks **DB-DMAC-MCn-AXI4-HT** SystemVerilog RTL IP Core is a high-throughput Scatter-Gather (SG) Direct Memory Access (DMA) Controller for AMBA AXI4 systems, with a build-time number of independent DMA Channels (1 to 126) and a DMA data path of 64 to 512 bits. It is the high-throughput member of the DB-DMAC-MC-AMBA family: a compatible register model, descriptor format and drivers, with a data engine rebuilt to keep the AXI4 bus full.

Writes run ahead of their data and go back-to-back, up to 16 reads and 16 writes are outstanding per channel, read data is never stalled, and the next descriptor node starts while the current one drains. Descriptor fetches and status write-back move to a dedicated AXI4 Manager, so they never wait behind DMA data. Measured at 128 bits, two channels use **97.6 %** of the bus, one channel holds **73 %** of the bus at a 200-cycle read latency, and a scatter-gather list pays **2 cycles** per descriptor node.

97.6 %	**73 %**	**2 cycles**	**100 %**
AXI4 bus use, 2 channels, 128-bit	AXI4 bus use, 1 channel, 200-cycle read latency	between descriptor nodes	branch / statement / FSM coverage, 0 protocol errors

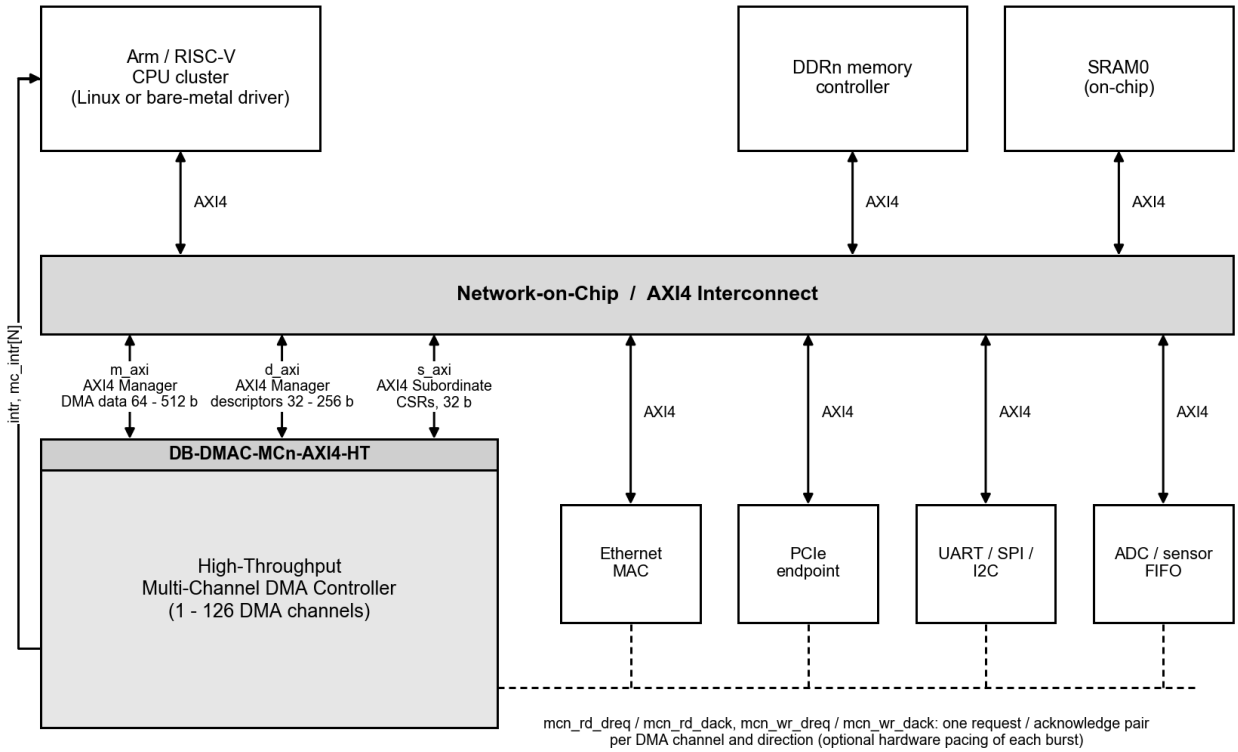


Figure 1: DB-DMAC-MCn-AXI4-HT in an SoC - memory-to-memory, memory-to-peripheral and peripheral-to-memory transfers over the NoC

Features

High-Throughput AXI4 Data Engine

- **Decoupled write path**: the write address (AW) is accepted into a 4-deep queue (2 to 16) as soon as it is granted; the write data (W) bursts follow in order, back-to-back. AWVALID and WVALID are independent (AXI4 channel key: see Interfaces)
- **Read-space reservation**: every beat of a read burst has its place reserved in the channel FIFO when the read address (AR) is issued - RREADY is constant 1, no head-of-line blocking between channels, any outstanding setting is safe with any burst length
- **Deep pipelining**: up to 16 outstanding reads and 16 outstanding write responses per channel; bursts of 4, 8, 16 or 1 to 256 beats
- **Descriptor overlap**: the next descriptor node's reads start once the current descriptor node's reads are issued; writes and completions stay in descriptor node order
- **Burst precompute**: each channel's next burst length and AxSIZE are computed a cycle ahead, off the arbitration path
- Round-robin channel arbitration with an O(log N) parallel-prefix select on each AXI4 Manager; per-channel ARQOS / AWQOS

Dedicated AXI4 Descriptor Manager

- Separate AXI4 port (d_axi) for descriptor fetches - fetches never queue behind DMA data
- Width 32 / 64 / 128 / 256 bits: a 32-byte descriptor node is one beat at 256 bits
- Per-channel pre-fetch of up to 32 descriptor nodes ahead of execution
- Optional **descriptor status write-back** into each descriptor node: off, failing node only, or every node - software scans the list without reading registers

Scatter-Gather and Transfer Control

- Linked lists of 32-byte descriptor nodes: 64-bit source, destination and next address, 24-bit byte length (1 byte to 16 MB per descriptor node)
- Chained and ring descriptor structures: list start / branch at any time, re-start (DLR) and Wait-On-Restart (WOR) for rings
- Memory-to-Memory, Memory-to-Peripheral, Peripheral-to-Memory, Peripheral-to-Peripheral
- Unaligned source and destination addresses at any byte, any length (byte rotator, WSTRB on the first and last word); automatic split at 4 KB boundaries
- Fixed-address (FIFO) reads and writes; hardware-paced bursts with per-channel DREQ / DACK pairs for reads and writes
- CPU software or external hardware initiated transfers

Status, Interrupts and Error Handling

- **Descriptor-level error reporting**: on the first error of a list the failing descriptor node's address is frozen and the cause is recorded (write response, read data or descriptor fetch; SLVERR or DECERR)
- Per-channel status with masks and interrupt outputs; global interrupt status / mask / vector registers and one processor interrupt
- Event-safe write-1-to-clear: a hardware event in the same cycle as the clear is never lost
- Optional per-byte parity checking on data and descriptor reads; parity generated on writes
- Self-describing Core Identification (CIR) and Core Feature (CFR) registers - drivers adapt to the build

Integration

- 1 to 126 channels (one global interrupt bank per 32); data width 64 / 128 / 256 / 512 bits; 64-bit addressing
- SystemVerilog interfaces with modports on the core, plus a flat-pin wrapper for synthesis and tool flows; AMBA AXI4 Manager / Subordinate naming (formerly Master / Slave)
- Elaboration-time checks reject illegal configuration values
- Fully synchronous single clock, rising-edge, no gated clocks, no internal tri-states; technology-independent RTL for ASIC and FPGA
- Build option without descriptor overlap: one descriptor node at a time

Applications

- Memory-to-memory copy engines in SoCs with high-latency DDR or HBM

- Scatter-gather DMA for networking, storage and PCIe endpoint data movement
- Peripheral data streaming with hardware request / acknowledge pacing
- Offload of bulk memory copies from CPU clusters, under Linux or bare metal

Architecture

Figure 2 shows the internal structure. Each DMA channel has its own registers, descriptor processor, 32-descriptor-node pre-fetch FIFO, control unit, read and write engines and a data FIFO. Three shared AXI4 Managers serve all channels: one for descriptors and two for DMA data reads and writes, each connected to the NoC's AXI4 channels (AR / R for reads, AW / W / B for writes). The numbered tags mark the high-throughput mechanisms.

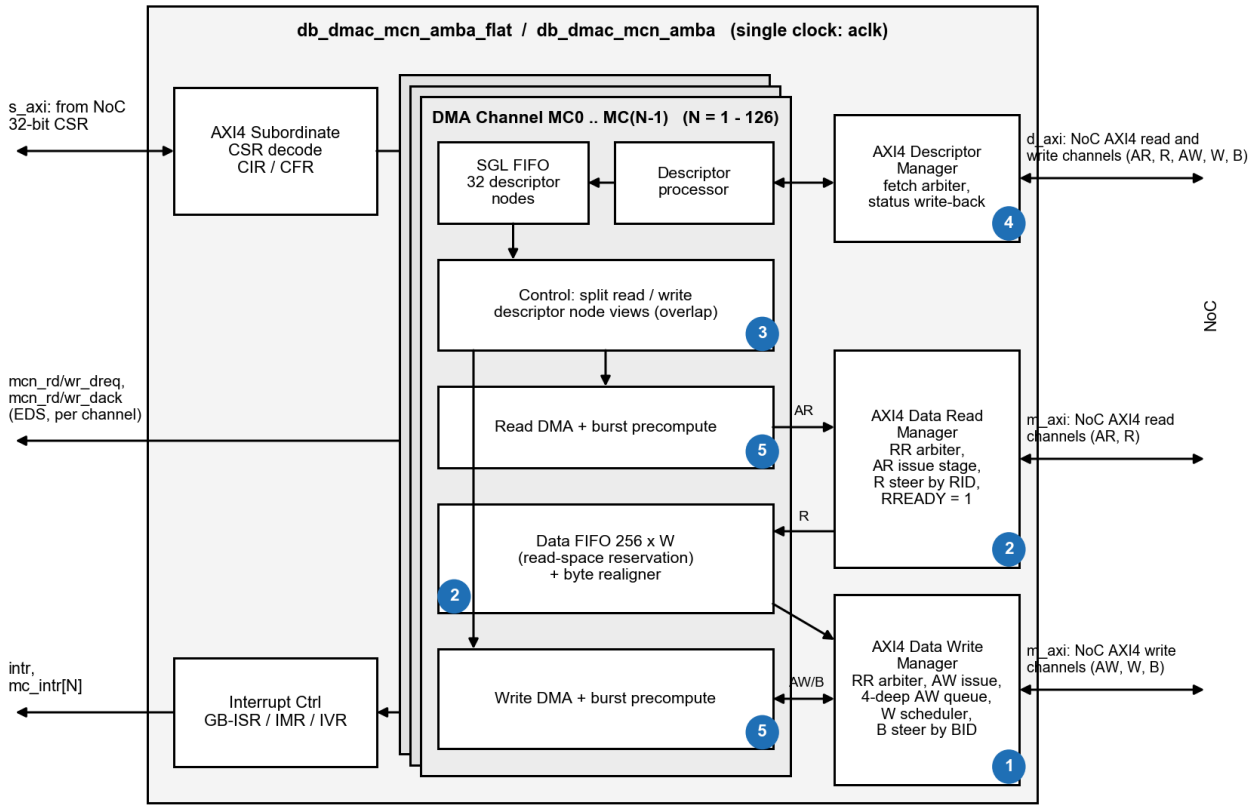


Figure 2: DB-DMAC-MCn-AXI4-HT internal architecture

#	Mechanism	What it removes
1	AW queue + W scheduler	The write path waiting for each write address (AW) handshake before its write data (W) burst; W bursts now stream back-to-back
2	Read-space reservation, RREADY = 1	Read stalls and head-of-line blocking between channels; FIFO overflow / deadlock risk with deep outstanding reads
3	Descriptor overlap	The idle gap at every descriptor node boundary (2 cycles remain)
4	Dedicated AXI4 descriptor manager	Descriptor fetches and status writes competing with DMA data on the same port
5	Burst precompute	Burst-length arithmetic on the arbitration / AR / AW path

Data flow: software writes the first descriptor node address and starts the channel. The descriptor processor fetches descriptor nodes over d_axi and queues them; the control unit loads the read and write engines; read bursts fill the data FIFO through m_axi, the realigner rotates bytes for unequal source / destination offsets and the write engine drains the FIFO. A descriptor node completes when its last write response is in, so its data is committed; the channel then updates its last-descriptor-node address, optionally writes the descriptor node's status word, and raises its completion interrupt.

Measured Performance

Cycle-accurate RTL simulation of the default build (128-bit AXI4 data manager, 16 bytes per cycle peak) against an AXI4 memory model with full-rate READY and programmable read and write-response latency; each scenario uses its best legal channel setting.

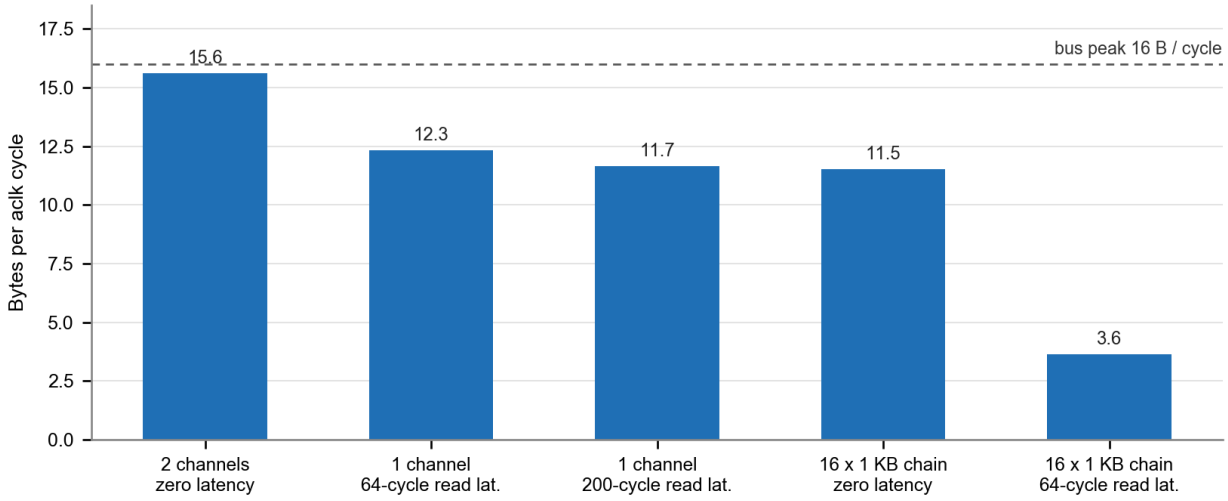


Figure 3: Measured throughput, 128-bit data path (bytes per aclk cycle)

Scenario	Conditions	Bytes / cycle	Bus use
Two channels in parallel, 64 KB each	16-beat bursts, zero memory latency	15.61	97.6 %
One channel, 64 KB copy	16-beat bursts, read latency 64, B latency 16, deepest outstanding setting	12.32	77.0 %
One channel, 64 KB copy	16-beat bursts, read latency 200, B latency 50, deepest outstanding setting	11.65	72.8 %
Scatter-gather chain of 16 x 1 KB descriptor nodes	16-beat bursts, zero memory latency	11.51	72.0 %
Scatter-gather chain of 16 x 1 KB descriptor nodes	read latency 64, B latency 16	3.65	22.8 %
Descriptor node boundary cost	16 x 1 KB descriptor nodes vs one 16 KB descriptor node, zero latency	2 cycles per boundary	-

At 200-cycle read latency one channel sustains 11.7 B / cycle with 16 reads outstanding (1.2 B / cycle with one outstanding) - deep outstanding reads are safe with any burst length because each read reserves its own FIFO space. Figures scale with the data width; results depend on the interconnect, memory and configuration. Evidence: doc/results/Rel_1_3_0 (perf_t1 - t3).

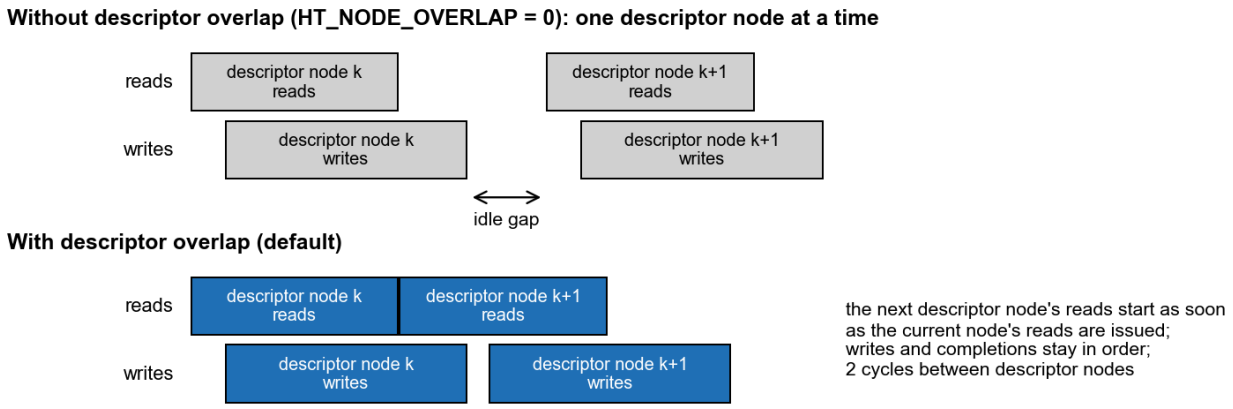


Figure 4: Descriptor overlap at a descriptor node boundary (illustrative, not to scale)

Interfaces

AMBA terminology used in this data sheet: an **AXI4 Manager** issues transactions (formerly 'AXI4 Master'); an **AXI4 Subordinate** responds to them (formerly 'AXI4 Slave'). The five AXI4 channels are abbreviated as follows:

Interface	Type	Width	Function
m_axi	AXI4 Manager (AR, R, AW, W, B)	Data 64 - 512 Address 64	DMA data reads and writes. INCR / FIXED bursts up to 256 beats, ID per channel, multiple outstanding transactions, read data interleaved across IDs, AxQOS, per-byte data parity
d_axi	AXI4 Manager (AR, R, AW, W, B)	Data 32 - 256 Address 64	Descriptor node fetches (ARID = channel) and single-beat descriptor status write-back
s_axi	AXI4 Subordinate	Data 32 Address 32	Control / status registers, 4 KB window, single-beat; SLVERR on unused or read-only offsets. Connects to AXI4-Lite through a bridge or simple tie-offs
mcn_rd_dreq / dack mcn_wr_dreq / dack	Request / acknowledge	1 per channel	Hardware pacing of individual read and write bursts by a peripheral (EDS-R / EDS-W)
intr, mc_intr[N]	Level interrupt	1 + N	Processor interrupt and per-channel interrupts
aclk, aresetn	Clock / reset	1, 1	Single clock; active-low reset, asynchronous assert, synchronous release
scan_mode	DFT	1	Holds the per-channel software reset inactive during scan

Verification

The DB-DMAC-MCn-AXI4-HT is delivered with the self-checking test bench used for sign-off. It programs the controller, sources and checks every transferred byte, and runs channel- and width-generic scenarios over every configured channel. AXI4 protocol checkers watch both AXI4 Managers in every test; any protocol assertion fails the test. Memory models inject wait states on every channel, programmable latency, read interleaving across IDs, SLVERR / DECERR and parity errors.

Deliverables

Item	Contents
RTL	Synthesizable SystemVerilog (IEEE 1800-2012), interface core and flat-pin wrapper; or a technology-specific netlist for FPGAs
Constraints / filelists	Synopsys Design Constraints, compile-ordered filelist, lint script and waivers
Test bench	Self-checking directed and generic suites, AXI4 memory models, AXI4 protocol checkers, regression driver with expected results and coverage scripts
Models	C++ cycle model build
Software	Bare-metal C driver with reference program; Linux platform driver, UAPI header and device-tree example
Documents	Data sheet, Technical Reference Manual, IP Integration Guide, coverage report, test matrix, regression evidence

Ordering Information

Digital Blocks offers a variety of methods for prospective customers to evaluate the DB-DMAC-MCn-AXI4-HT. Please contact Digital Blocks for additional technical, pricing, evaluation and support information. An AXI5 high-throughput variant (DB-DMAC-MCn-AXI5-HT) is available.

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