Digital Blocks

Semiconductor IP

DB-DMAC-MCn-AXI5-HT

High-Throughput Multi-Channel DMA Controller

Scatter-Gather | AMBA AXI5 | 1 - 126 Channels

General Description

The Digital Blocks **DB-DMAC-MCn-AXI5-HT** SystemVerilog RTL IP Core is a high-throughput Scatter-Gather (SG) Direct Memory Access (DMA) Controller with AMBA AXI5 Manager interfaces, a build-time number of independent DMA Channels (1 to 126) and a DMA data path of 64 to 1024 bits. It adds the AXI5 throughput features - unique IDs with out-of-order completion, read data chunking, the Busy indicator, QoS Accept and Max_Transaction_Bytes - to the DB-DMAC-MCn-AXI4-HT engine, so the interconnect and memory can keep up with a controller that already runs close to the full bus rate.

The inherited engine is measured: at 128 bits two channels use **97.6 %** of the AXI4 bus, one channel holds **73 %** at a 200-cycle read latency, and descriptor nodes are **2 cycles** apart. The AXI5-HT keeps those mechanisms and lifts the limits that remain: one data ID per channel becomes a pool of unique IDs, so a channel's reads and writes complete out of order; wide reads come back in 128-bit chunks in any order; and the outstanding limit and channel arbitration follow the interconnect's Busy and QoS Accept signals. Every AXI5 feature is a build or register option; with all of them off the core behaves as the DB-DMAC-MCn-AXI4-HT.

1024-bit	16 IDs	97.6 %	AXI4-HT
data path option (64 to 1024 bits)	unique AXI IDs per channel, out-of-order completion	bus use of the inherited AXI4-HT engine (measured)	behavior with every AXI5 option off

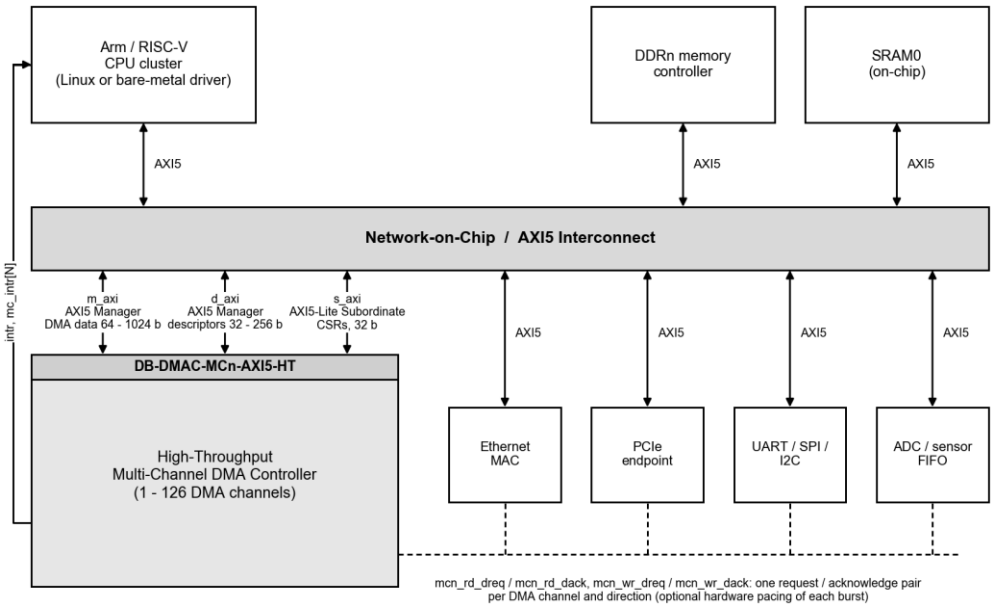


Figure 1: DB-DMAC-MCn-AXI5-HT in an SoC - memory-to-memory, memory-to-peripheral and peripheral-to-memory transfers over the NoC

Features

High-Throughput Engine (from DB-DMAC-MCn-AXI4-HT, measured)

- **Decoupled write path**: AW runs ahead of W through a queue; W bursts go back-to-back
- **Read-space reservation**: buffer space is claimed when a read is issued, so RREADY is constant 1 - no read stalls, no head-of-line blocking between channels
- **Descriptor overlap**: the next node's reads start while the current node's writes drain (2 cycles between nodes)
- **Dedicated descriptor manager** with optional descriptor status write-back into each node
- Up to 16 outstanding reads and 16 outstanding writes per channel; burst lengths computed a cycle ahead, off the arbitration path

AXI5 Throughput Features

- **Unique ID indicator**: every burst takes its own ID from a per-channel pool (1 to 16, default 8) and asserts AxIDUNQ - the interconnect needs no ordering tracking for it
- **Out-of-order completion**: one channel's reads and writes complete in any order; data is reordered in a slot buffer and completion is counted per descriptor
- **Read data chunking**: memory returns wide reads in 128-bit chunks in any order; each chunk is written straight into its buffer slot
- **Busy indicator**: the outstanding-transaction limit steps down with RBUSY / BBUSY (75 / 50 / 25 %) and recovers after a hold-off
- **QoS Accept**: the round-robin arbiter favors requests the subordinate will accept now
- **Max_Transaction_Bytes**: bursts are cut at the interconnect stripe size (64 to 4096 bytes), so the interconnect never splits them
- **Wake-up**: AWAKEUP is raised a cycle before the first request after idle

AXI5 Transactions

- **WriteZero** zero fill per node: no source read and no write data on the bus
- **WriteNoSnoopFull**: full-line, all-strobe writes let a system cache allocate without merging
- **Prefetch**: optional data-less hint issued ahead of the read stream to hide DRAM latency
- Regular-transactions-only build for interconnects that require it

System, Integrity and Control

- Per-channel ARCACHE / AWCACHE and ARPROT / AWPROT: bufferable writes allow early responses; no-allocate reads keep source data out of the system cache
- **Data Check**: odd parity per byte on read and write data (RDATACHK / WDATACHK)
- AXI5-Lite register subordinate with WSTRB; 32-bit, 4 KB register window
- Descriptor-level error reporting: failing node address and cause (write response, read data or descriptor fetch; SLVERR or DECERR)
- Per-channel status and interrupts, global interrupt status / mask / vector, one processor interrupt; CIR and CFR describe the build to software

Scatter-Gather and Transfer Control

- Linked lists of 32-byte nodes with 64-bit addresses and a 24-bit length; chained and ring structures (start / branch, re-start, Wait-On-Restart)
- Memory-to-Memory, Memory-to-Peripheral, Peripheral-to-Memory, Peripheral-to-Peripheral; fixed-address FIFO transfers; per-channel DREQ / DACK hardware pacing
- Unaligned source and destination at any byte, any length

Integration

- 1 to 126 channels (one global interrupt bank per 32); data width 64 / 128 / 256 / 512 / 1024 bits; 64-bit addressing
- Each AXI5 feature is a build or register option, declared through the AXI5 interface properties; with all off the core is the DB-DMAC-MCn-AXI4-HT
- SystemVerilog interfaces with modports plus a flat-pin wrapper; AMBA Manager / Subordinate naming
- Fully synchronous single clock, rising-edge, no gated clocks, no internal tri-states; technology-independent RTL for ASIC and FPGA

Applications

- Bulk data movement on AXI5 network-on-chip and mesh interconnects with DDR or HBM memory
- Wide 512 and 1024-bit data paths where read latency dominates
- Buffer initialization and zero fill without a source read
- Scatter-gather DMA for networking, storage and PCIe endpoint data movement

Architecture

Figure 2 shows the internal structure. The channel cores and the three shared managers are those of the DB-DMAC-MCn-AXI4-HT; the AXI5-HT replaces each channel's data FIFO with a slot buffer and adds a unique-ID pool and AXI5 flow control to the data managers. Grey tags mark mechanisms already in the AXI4-HT; blue tags mark what AXI5 adds.

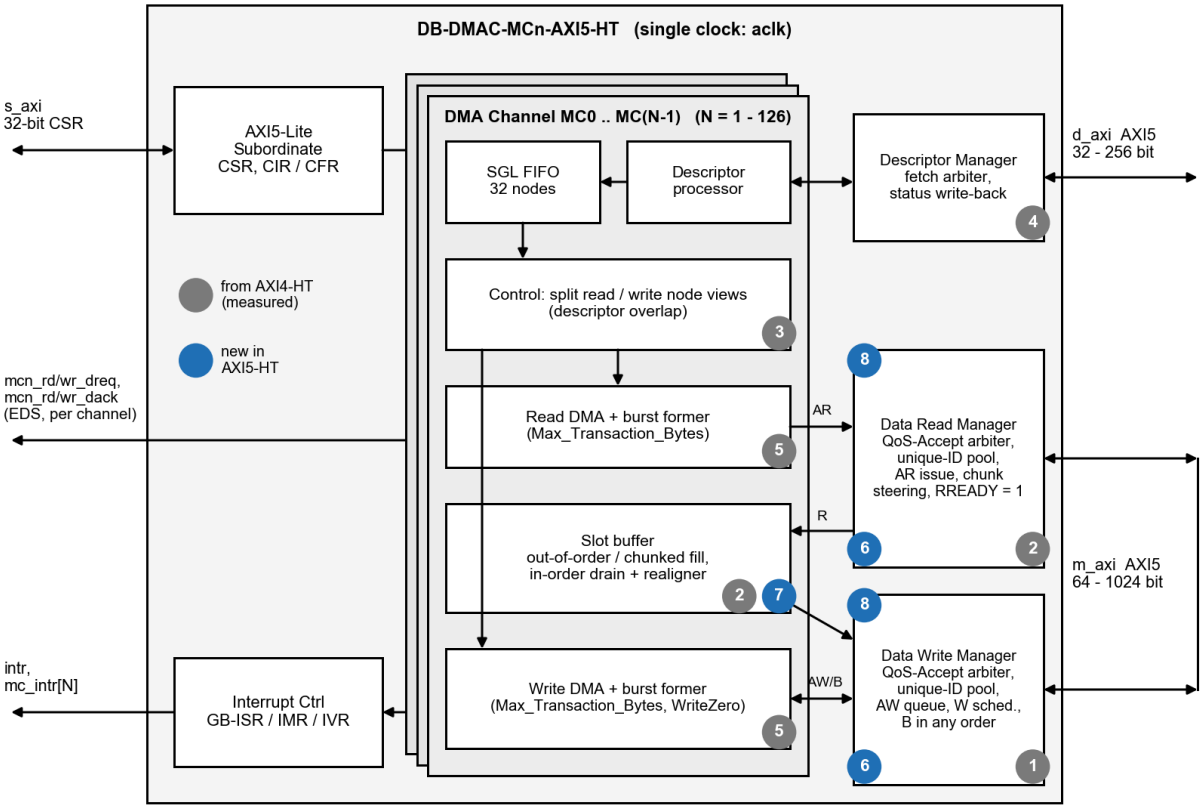


Figure 2: DB-DMAC-MCn-AXI5-HT internal architecture

#	Mechanism	Status	What it does
1	AW queue + W scheduler	AXI4-HT	W bursts stream back-to-back; AW runs ahead
2	Read-space reservation, RREADY = 1	AXI4-HT	No read stalls or head-of-line blocking; any outstanding depth is safe
3	Descriptor overlap	AXI4-HT	Node boundary 24 -> 2 cycles
4	Dedicated descriptor manager	AXI4-HT	Descriptor traffic never waits behind DMA data
5	Burst former	AXI4-HT + AXI5	Lengths computed off the grant path; cut at Max_Transaction_Bytes; WriteZero form
6	Unique-ID pool	AXI5	Each burst its own ID with AxIDUNQ; a channel's reads and writes complete out of order
7	Slot buffer	AXI5	Out-of-order and chunked R fill; in-order drain through the byte realigner
8	Busy / QoS-Accept arbitration	AXI5	Outstanding limit follows RBUSY / BBUSY; arbiter favors requests the subordinate accepts now

Performance

The AXI5-HT data engine is the DB-DMAC-MCn-AXI4-HT engine. Figure 3 shows that engine measured in cycle-accurate RTL simulation at 128 bits (16 bytes per cycle peak), against the DB-DMAC-MCn-AXI4 it replaced. AXI5-HT figures will be published from its own performance tests.

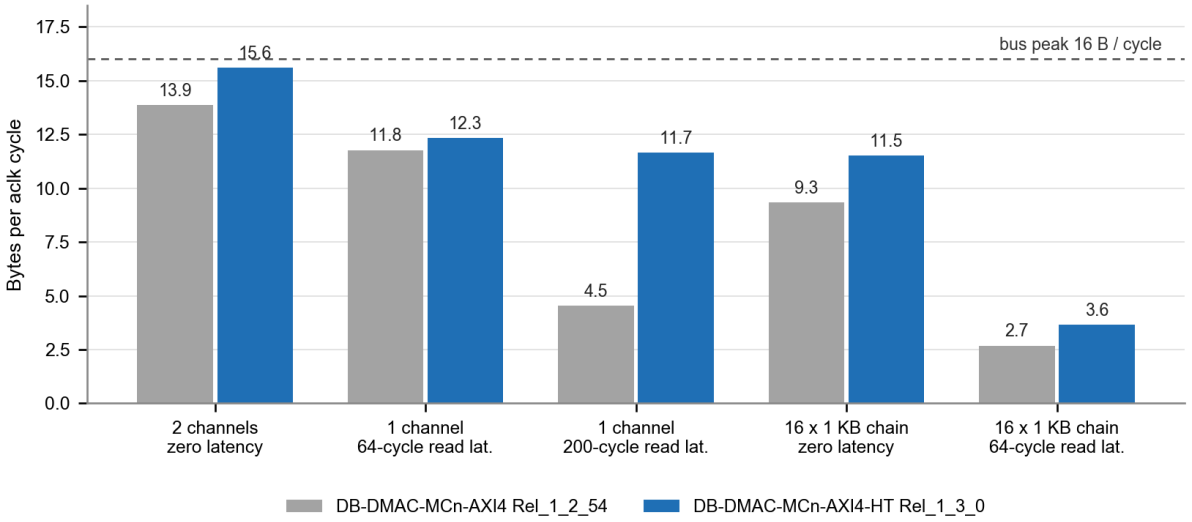


Figure 3: Measured throughput of the inherited AXI4-HT engine, 128-bit (bytes per aclk cycle)

What AXI5 Adds

AXI5 feature	Expected effect (engineering estimate, to be measured)
Unique IDs, out-of-order completion	A slow memory region no longer holds up a channel's later bursts; responses complete as the memory delivers them
Read data chunking	Wide-bus read latency cut by the memory's own chunk reordering
Busy indicator, QoS Accept	Fewer interconnect stalls under load; requests go where they are accepted now
Max_Transaction_Bytes	No interconnect splitting of DMA bursts
1024-bit data path	Twice the bytes per beat of the 512-bit build
WriteZero	Zero fill with no read bandwidth and no write-data bandwidth

Buffer Sizing for Full Read Rate

To keep the read channel busy, a channel needs as many beats in flight as the read latency in cycles (Little's law). The slot buffer holds those beats plus one write burst:

Read latency	Beats in flight	16-beat bursts outstanding	Buffer at 512 bits	Buffer at 1024 bits
64 cycles	64	4	4 KiB + 1 KiB	8 KiB + 2 KiB
128 cycles	128	8	8 KiB + 1 KiB	16 KiB + 2 KiB
256 cycles	256	16	16 KiB + 1 KiB	32 KiB + 2 KiB

Interfaces

Interface	Type	Width	Function
m_axi	AXI5 Manager (AR, R, AW, W, B)	Data 64 - 1024 Address 64	DMA data reads and writes: INCR / FIXED bursts up to 256 beats, unique IDs, out-of-order completion, chunked read data, Busy and QoS Accept flow control, AxQOS / AxCACHE / AxPROT, AWAKEUP, AWSNOOP, data check
d_axi	AXI5 Manager (AR, R, AW, W, B)	Data 32 - 256 Address 64	Descriptor node fetches and single-beat status write-back
s_axi	AXI5-Lite Subordinate	Data 32 Address 32	Control / status registers with WSTRB, 4 KB window
mcn_rd_dreq / dack mcn_wr_dreq / dack	Request / acknowledge	1 per channel	Hardware pacing of individual read and write bursts by a peripheral
intr, mc_intr[N]	Level interrupt	1 + N	Processor interrupt and per-channel interrupts
aclk, aresetn, scan_mode	Clock / reset / DFT	1, 1, 1	Single clock; active-low reset; scan-mode override of the channel software reset

Declared AXI5 Interface Properties

Property	Declared value	If the subordinate does not support it
Unique_ID_Support	True	Signals left unconnected; no functional change
Read_Data_Chunking	True (build option)	Data returns in order; the slot buffer handles both
Max_Transaction_Bytes	64 - 4096 (build option)	Set no greater than the subordinate's value
Busy_Support	True (build option)	Inputs tied 00: the outstanding limit stays at maximum
QoS_Accept	True (build option)	Inputs tied 0000: plain round robin
WriteZero_Transaction	True (build option)	Build with WriteZero off; zero fill uses the data path
Regular_Transactions_Only	Build option	A True manager connects anywhere
Check_Type	Odd_Parity_Byte_All (build option)	Check signals left unconnected
Ordered_Write_Observation	Not required	Completion is tracked per descriptor from B

Verification

The inherited engine is signed off in DB-DMAC-MCn-AXI5-HT Rel_1_3_0: 40 / 40 tests in the default build and every test in 13 channel-count, data-width and descriptor-width sweep builds pass, with 100 % branch, statement and FSM coverage and AXI5 protocol checkers on both managers in every test.

Not Included (as of this publication)

Atomic transactions, memory tagging, cache stashing, untranslated transactions and SMMU hints, WriteDeferrable, write-plus-CMO, trace, loopback, MPAM, Realm and Poison do not move bulk data faster or need a coherent system. Cache stashing and untranslated transactions are the first candidates for a later release.

Deliverables

Item	Contents
RTL	Synthesizable SystemVerilog (IEEE 1800-2012), interface core and flat-pin wrapper; or a technology-specific netlist for FPGAs
Constraints / filelists	Synopsys Design Constraints, compile-ordered filelist, lint script and waivers
Test bench	Self-checking directed and generic suites, AXI5 memory models, AXI5 protocol checkers, regression driver with expected results and coverage scripts
Models	C++ cycle model build
Software	Bare-metal C driver with reference program; Linux platform driver, UAPI header and device-tree example
Documents	Data sheet, Technical Reference Manual, IP Integration Guide, coverage report, test matrix, regression evidence

Ordering Information

Digital Blocks offers a variety of methods for prospective customers to evaluate the DB-DMAC-MCn-AXI5-HT. Please contact Digital Blocks for additional technical, pricing, evaluation and support information. An AXI4 high-throughput variant (DB-DMAC-MCn-AXI4-HT) is available.

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