General Description

The Digital Blocks DB-I2C-M-AHB Controller IP Core interfaces an ARM, MIPS, PowerPC, ARC or other high performance microprocessor via the AMBA 2.0 AHB System Interconnect Fabric to an I2C Bus. The I2C is a two-wire bidirectional interface standard (SCL is Clock, SDA is Data) for transfer of bytes of information between two or more compliant I2C devices, typically with a microprocessor behind the master controller and one or more slave devices.

The DB-I2C-M-AHB is a Master I2C Controller that controls the Transmit or Receive of data to or from slave I2C devices. Figure 1 depicts the system view of the DB-I2C-M-AHB Controller IP Core embedded within an integrated circuit device.

The DB-I2C-M-AHB Controller IP Core targets embedded processor applications with higher performance algorithm requirements. While most I2C controllers require high processor interaction involvement, the DB-I2C-M-AHB contains a parameterized FIFO and Finite State Machine control for the processor to off-load the I2C transfer to the DB-I2C-M-AHB Controller. Thus, while the DB-I2C-M-AHB is busy, independently controlling the I2C Transmit or Receive transaction of data, the processor can go off and complete other tasks. Note that the Master only capability of the DB-I2C-M-AHB adds to its small VLSI footprint requirements.
Features

- Master I²C Controller Modes:
  - Master – Transmitter
  - Master – Receiver
- Supports four I²C bus speeds:
  - High-Speed Mode (3.4+ Mb/s)
  - Fast Mode Plus (1 Mbit/s)
  - Fast Mode (400 Kb/s)
  - Standard Mode (100 Kb/s)
- Parameterized FIFO memory for off-loading the I²C transfers from the processor:
  - Targets embedded processors with higher performance algorithm requirements, by the I²C Controller independently controlling the Transmit or Receive of bytes of information buffered to and from a FIFO.
- Enhanced system-level features & integration capabilities:
  - CPU Interface via parameterized FIFO with support for APB / AHB / AXI / AXI-lite / Avalon / Qsys interconnect fabrics
  - Enhanced SCL / SDA spike filtering capabilities
  - Enhanced Repeated Start capabilities
- Enhanced system-level features & integration capabilities (Optional):
  - DMA transfer between the I2C Bus & Memory (SDRAM / SRAM / FLASH)
  - Direct interface to user Registers within ASIC / ASSP / FPGA device, for Master/Slave transfer across the I2C Bus
  - Remote Configuration of a Digital Blocks’ I2C Slave by an I2C Master
- I²C compliant features:
  - Multi-Master, Clock Synchronization, Arbitration, Repeated Start, 7/10-bit addressing, & General Call Addressing
- 13 sources of internal interrupts with masking control
- Compliance with AMBA 2.0 and I²C specifications:
  - AMBA Specification (Rev 2.0), AHB Bus
- Fully-synchronous, synthesizable Verilog or VHDL RTL core, with rising-edge clocking, no gated clocks, and no internal tri-states, for easy integration into FPGA or ASIC design flows.

Digital Blocks offers I2C Master/Slave, Master-only, and Slave-only Controller IP supporting Hs-Mode / Fast Mode Plus / Fast Mode / Standard Mode.
**Pin Description**

In addition to the AMBA AHB Bus interfaces, which include the input CLOCK and
RESET signals and the output INTR (interrupt) signal, the I2C interface signals are listed
in Table 1.

<table>
<thead>
<tr>
<th>Name</th>
<th>Type</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>SDAi</td>
<td>Input</td>
<td>Serial Data</td>
</tr>
<tr>
<td>SDAO</td>
<td>Output</td>
<td>Serial Data</td>
</tr>
<tr>
<td>SCL0</td>
<td>Output</td>
<td>Serial Clock Line</td>
</tr>
</tbody>
</table>

*Table 1: DB-I2C-M-AHB – I/O Pin Description*

**Verification Method**

The DB-I2C-M-AHB Controller IP Core contains a test suite with AHB Bus functional
models that program the DB-I2C-M-AHB control & status registers, generates & sends
I2C data, monitors the I2C bus protocol, and checks expected results.

The DB-I2C-M-AHB Controller IP Core has been verified as follows:

- Instantiated within an FPGA, controlled by a processor, and communicating with
  (1) a merchant semiconductor device containing an I2C Slave bus interface;
  and (2) an ASIC containing an I2C Slave bus interface

**Customer Evaluation**

Digital Blocks offers a variety of methods for prospective customers to evaluate the DB-I2C-M-AHB. Please contact Digital Blocks for additional information.

**Deliverables**

The DB-I2C-M-AHB is available in synthesizable RTL Verilog or VHDL or a
technology-specific netlist for FPGAs, along with synthesis scripts, a simulation test
bench with expected results, datasheet, and user manual.
Ordering Information

Please contact Digital Blocks for additional technical, pricing, evaluation, and support information.

Digital Blocks, Inc.
PO Box 192
587 Rock Rd
Glen Rock, NJ 07452 USA
Phone: +1-201-251-1281
eFax: +1-702-552-1905
info@digitalblocks.com

Copyright © Digital Blocks, Inc. 2007 - 2018, ALL RIGHTS RESERVED

###
Digital Blocks is a registered trademark of Digital Blocks, Inc.
All other trademarks are the property of their respective owners