Digital Blocks
Semiconductor IP

DB-I2C-M-Hs-Mode
Hs-Mode I2C Master Controller

General Description

The Digital Blocks DB-I2C-M-Hs-Mode Controller IP Core interfaces a microprocessor via the AMBA AXI / AHB / APB Bus or Avalon Bus to an I2C Bus in Hs-Mode (3.4 Mbit/s) / Fast-Mode Plus (1 Mbit/s) / Fast-Mode (400 Kbit/s) / Standard-Mode (100 Kbit/s). The DB-I2C-M-Hs-Mode Controller IP Core can also interface a set of Registers within an ASIC / ASSP / FPGA device as well as interface Memory (e.g. SDRAM / SRAM / FLASH) to an I2C Bus.

The I2C is a two-wire bidirectional interface standard (SCL is Clock, SDA is Data) for transfer of bytes of information between two or more compliant I2C devices, typically with a microprocessor behind the master controller and one or more slave devices.

The DB-I2C-M-Hs-Mode is a Master I2C Controller that controls the Transmit or Receive of data to or from slave I2C devices. Figure 1 depicts the system view of the DB-I2C-M-AHB Controller IP Core embedded within an integrated circuit device.

In an ASIC / ASSP / FPGA integrated circuit, typically, the microprocessor is an ARM processor, but can be any embedded processor. Figure 1 depicts the system view of the DB-I2C-M-Hs-Mode Controller IP Core embedded within an integrated circuit device with its Microprocessor Configuration.

Figure 1: DB-I2C-M-Hs-Mode Controller – System Diagram

The DB-I2C-M-Hs-Mode Controller IP Core targets embedded processor applications with higher performance algorithm requirements. While most I2C controllers require high processor interaction involvement, the DB-I2C-M-Hs-Mode contains a
parameterized FIFO and Finite State Machine Control for the processor to off-load the I2C transfer to the DB-I2C-M-Hs-Mode Controller. Thus, while the DB-I2C-M-Hs-Mode is busy, independently controlling the I2C Master-Transmit or Master-Receive transaction of data, the processor can complete other tasks. All Master Transmit / Receive transfers are with respect to the internal FIFO, thus fully isolating the processor from the I2C transfer of a block of data.

Features

- Master I2C Controller Modes:
  - Master – Transmitter
  - Master – Receiver

- Supports four I2C bus speeds:
  - Hs-Mode (3.4+ Mb/s)
  - Fast Mode Plus (1 Mbit/s)
  - Fast Mode (400 Kb/s)
  - Standard Mode (100 Kb/s)

- Parameterized FIFO memory for off-loading the I2C transfers from the processor:
  - Targets embedded processors with higher performance algorithm requirements, by the I2C Controller independently controlling the Transmit or Receive of bytes of information buffered to and from a FIFO.

- Enhanced system-level features & integration capabilities:
  - CPU Interface via parameterized FIFO with support for APB / AHB / AXI / AXI-lite / Avalon / Qsys interconnect fabrics
  - Enhanced SCL / SDA spike filtering capabilities
  - Enhanced Repeated Start capabilities

- Enhanced system-level features & integration capabilities (Optional):
  - DMA transfer between the I2C Bus & Memory (SDRAM / SRAM / FLASH)
  - Direct interface to user Registers within ASIC / ASSP / FPGA device, for Master/Slave transfer across the I2C Bus
  - Remote Configuration of a Digital Blocks’ I2C Slave by an I2C Master

- I2C compliant features:
  - Multi-Master, Clock Synchronization, Arbitration, Repeated Start, 7/10-bit addressing, & General Call Addressing, Hs-Mode

- 13 sources of internal interrupts with masking control

- Compliance with AMBA and I2C specifications:
  - Compliance with AMBA AXI / AHB/ APB Protocol Specifications
  - Compliance with Avalon / Qsys Protocol Specifications
Fully-synchronous, synthesizable Verilog RTL core, with rising-edge clocking, no gated clocks, and no internal tri-states, for easy integration into FPGA or ASIC design flows.

Digital Blocks offers I2C Master/Slave, Master-only, and Slave-only Controller IP supporting Hs-Mode / Fast Mode Plus / Fast Mode / Standard Mode.

**Pin Description**

In addition to the AMBA AXI Bus interfaces, which include the input CLOCK and RESET signals and the output INTR (interrupt) signal, the I2C interface signals are listed in Table 1.

<table>
<thead>
<tr>
<th>Name</th>
<th>Type</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>SDAI</td>
<td>Input</td>
<td>Serial Data</td>
</tr>
<tr>
<td>SDAO</td>
<td>Output</td>
<td>Serial Data</td>
</tr>
<tr>
<td>SCLI</td>
<td>Input</td>
<td>Serial Clock Line</td>
</tr>
<tr>
<td>SCLO</td>
<td>Output</td>
<td>Serial Clock Line</td>
</tr>
</tbody>
</table>

**Table 1: DB-I2C-M-Hs-Mode – I/O Pin Description**

**Verification Method**

The DB-I2C-M-Hs-Mode Controller IP Core contains a test suite with AMBA AXI / AHB / APB Bus or Avalon / Qsys Bus functional models that program the DB-I2C-M-Hs-Mode control & status registers, generates & sends I2C data, monitors the I2C bus protocol, and checks expected results.

The DB-I2C-M-Hs-Mode Controller IP Core has internally been verified as follows:

- Instantiated within an FPGA, controlled by an ARM processor, and communicating with (1) merchant semiconductor devices containing an I2C Slave bus interface; and (2) ASICs containing I2C Slave bus interface

**Customer Evaluation**

Digital Blocks offers a variety of methods for prospective customers to evaluate the DB-I2C-M-Hs-Mode. Please contact Digital Blocks for additional information.

**Deliverables**

The DB-I2C-M-Hs-Mode is available in synthesizable RTL Verilog or a technology-specific netlist for FPGAs, along with Synopsys Design Constraints, a simulation test bench with expected results, datasheet, and user manual.
The DB-I2C-M-Hs-Mode comes along with example C code software for controlling Transmit and Receive Transactions in an Eclipse-based ARM Integrated Development Environment (IDE).

**Ordering Information**

Please contact Digital Blocks for additional technical, pricing, evaluation, and support information.

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