

## General Description

The Digital Blocks DB-I2C-MS-APB Controller IP Core interfaces a microprocessor via the AMBA APB Bus to an I2C Bus in Standard-Mode (100 Kbit/s) / Fast-Mode (400 Kbit/s) / Fast-Mode Plus (1 Mbit/s) / Hs-Mode (3.4+ Mb/s) / Ultra Fast-Mode (5 mbit/s).

The I2C is a two-wire bidirectional interface standard (SCL is Clock, SDA is Data) for transfer of bytes of information between two or more compliant I2C devices, typically with a microprocessor behind the master controller and one or more slave devices.

The DB-I2C-MS-APB is a Master/Slave I2C Controller that in Master Mode controls the Transmit or Receive of data to or from slave I2C devices while in Slave Mode allows an external I2C Master device to control the Transmit or Receive of data.

In an ASIC / ASSP / FPGA integrated circuit, typically, the microprocessor is an ARM processor, but can be any embedded processor. Figure 1 depicts the system view of the DB-I2C-MS-APB Controller IP Core embedded within an integrated circuit device with its Microprocessor Configuration.

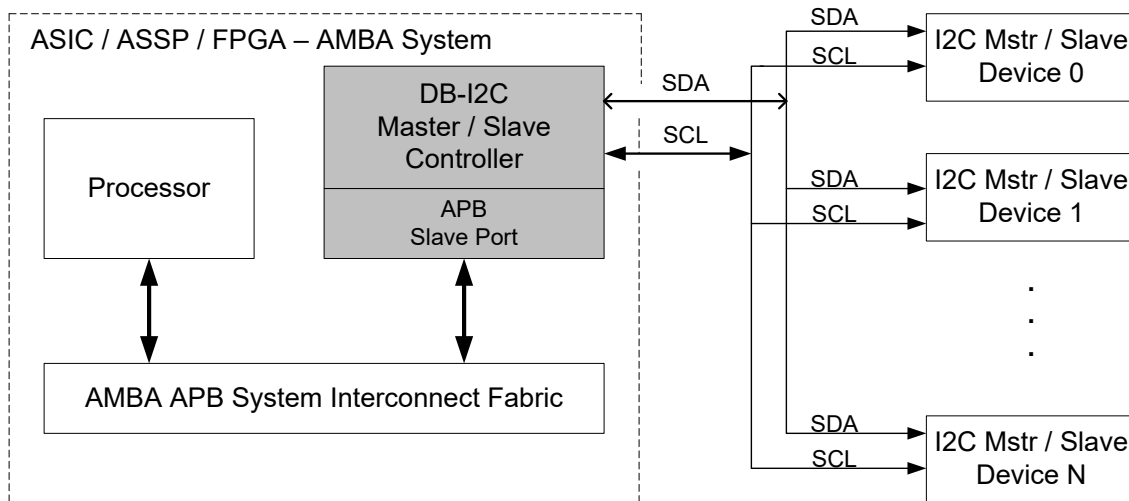


Figure 1: DB-I2C-MS-APB Controller – System Diagram

The DB-I2C-MS-APB Controller IP Core targets embedded processor applications with higher performance algorithm requirements as well as I2C transfer requirements to a set of Registers or Memory. While most I2C controllers require high processor interaction involvement, the DB-I2C-MS-APB contains a parameterized FIFO and Finite State Machine Control for the processor to off-load the I2C transfer to the DB-I2C-MS-APB Controller. Thus, while the DB-I2C-MS-APB in Master Mode is busy, independently

controlling the I2C Transmit or Receive transaction of data, or in Slave Mode, allowing the external I2C Master device to control the Transmit or Receive of data, the processor can complete other tasks. All Master & Slave Mode Transmit / Receive transfers are with respect to the internal FIFO, thus fully isolating the processor from the I2C transfer of a block of data.

## Features

- Master / Slave I<sup>2</sup>C Controller Modes:
  - Master – Transmitter
  - Master – Receiver
  - Slave – Transmitter
  - Slave – Receiver
- Supports following I2C bus speeds:
  - Hs-Mode (3.4+ Mb/s)
  - Ultra Fast-Mode (5 Mbit/s)
  - Fast Mode Plus (1 Mbit/s)
  - Fast Mode (400 Kb/s)
  - Standard Mode (100 Kb/s)
- I2C compliant features:
  - Clock Synchronization, Arbitration, SCL held low by Slave, Repeated Start, 7/10-bit addressing, & General Call
- Parameterized FIFO memory for off-loading the I<sup>2</sup>C transfers from the processor:
  - Targets embedded processors with higher performance algorithm requirements, by the I<sup>2</sup>C Controller independently controlling the Transmit or Receive of bytes of information buffered to and from a FIFO.
- System-level features & integration capabilities:
  - CPU Interface via parameterized FIFO with support for APB / AHB / AXI / AXI-lite / Avalon SoC Interconnect fabrics
  - Enhanced SCL / SDA spike filtering capabilities
  - Enhanced Repeated Start capabilities
- Optional system-level features & integration capabilities:
  - DMA transfer between the I2C Bus & Memory (SDRAM / SRAM / FLASH)
  - Direct interface to user Registers within ASIC / ASSP / FPGA device, for Master/Slave transfer across the I2C Bus
  - Remote Configuration of a Digital Blocks' I2C Slave by an I2C Master
  - SMBus Support:
    - SMBCLK Clock Low Timeout
    - SMBDAT minimum data hold time
- 13 sources of internal interrupts with masking control
- Compliance with AMBA and I2C specifications:
  - Compliance with AMBA Specification 2.0 – APB

- Philips/NXP – The I2C-Bus Specification, Version 2.1, January 2000 and UM10204 Rev 7 – 1 Oct 2021
- Fully-synchronous, synthesizable Verilog or VHDL RTL core, with rising-edge clocking, no gated clocks, and no internal tri-states, for easy integration into FPGA or ASIC design flows.

## Pin Description

In addition to the AMBA APB Bus interfaces, which include the input CLOCK and RESET signals and the output INTR (interrupt) signal, the I2C interface signals are listed in Table 1.

Name	Type	Description
<b>I2C Bus interface</b>		
SDAI	Input	Serial Data
SDAO	Output	Serial Data
SCLI	Input	Serial Clock Line
SCLO	Output	Serial Clock Line

**Table 1: DB-I2C-MS-APB – I/O Pin Description**

## Verification Method

The DB-I2C-MS-APB Controller IP Core contains a verification test suite with AMBA APB Bus functional models that program the DB-I2C-MS-APB control & status registers, generates & sends I2C data, monitors the I2C bus protocol and timing, and checks expected results.

The DB-I2C-MS-APB Controller IP Core has internally been verified as follows:

- Instantiated within an FPGA, controlled by an ARM processor, and communicating with (1) I2C Master and I2C Slave merchant semiconductor devices, including devices from NXP; and (2) variety of ASICs containing I2C Master & Slave bus interfaces

## Customer Evaluation

Digital Blocks offers a variety of methods for prospective customers to evaluate the DB-I2C-MS-APB. Please contact Digital Blocks for additional information.

## Deliverables

The DB-I2C-MS-APB is available in synthesizable RTL Verilog a technology-specific netlist for FPGAs, along with Synopsys Design Constraints, a simulation test bench with expected results, datasheet, and user manual.

The DB-I2C-MS-APB comes along with example C code software for controlling Transmit and Receive Transactions in an Eclipse-based ARM Integrated Development Environment (IDE).

## Ordering Information

Please contact Digital Blocks for additional technical, pricing, evaluation, and support information.

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