Digital Blocks
Semiconductor IP

DB-I2C-SMBUS-MS-AXI
DB-I2C-SMBUS-MS-AHB
DB-I2C-SMBUS-MS-APB
AMBA Bus I2C-SMBus Controller

General Description

The Digital Blocks DB-I2C-SMBus-MS-AMBA Controller IP Core is an I2C/SMBus Master/Slave Controller, interfacing a microprocessor via the AMBA AXI, AHB, or APB Bus to an I2C/SMBus Interconnect. Both I2C and SMBus protocols are supported.

The I2C/SMBus is a two-wire bidirectional interface standard (SCL is Clock, SDA is Data) for transfer of bytes of information between two or more compliant I2C devices, typically with a microprocessor behind the master controller and one or more slave devices.

The DB-I2C-SMBus-MS-AMBA is a Master/Slave I2C Controller that in Master Mode controls the Transmit or Receive of data to or from slave I2C/SMBus devices while in Slave Mode allows an external I2C/SMBus Master device to control the Transmit or Receive of data.

In an ASIC / ASSP / FPGA integrated circuit, typically, the microprocessor is an ARM processor, but can be any embedded processor. Figure 1 depicts the system view of the DB-I2C-SMBus-MS-AMBA Controller IP Core embedded within an integrated circuit device with its Microprocessor Configuration.

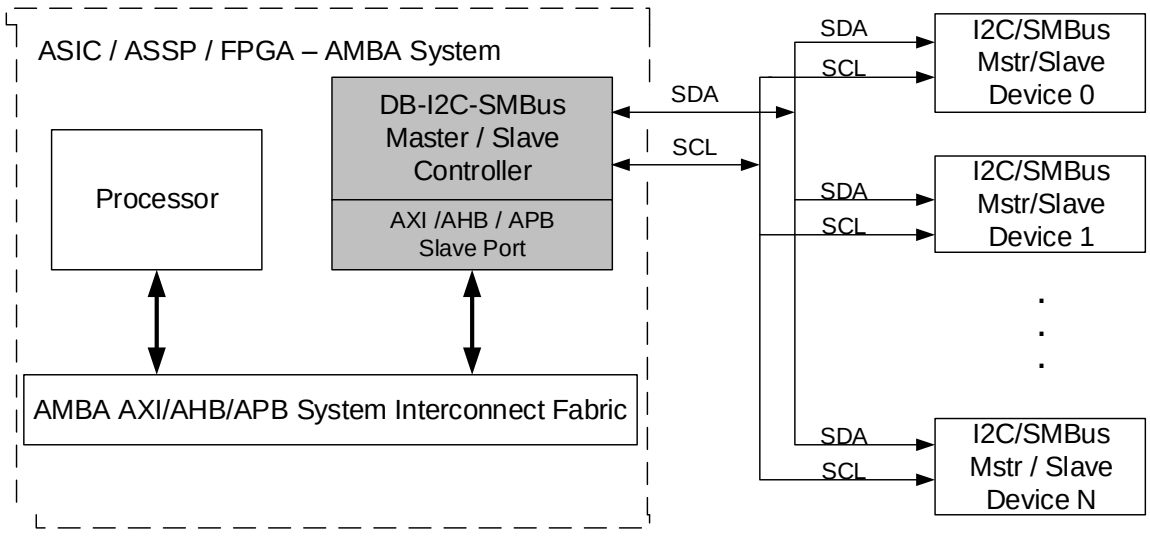

Figure 1: DB-I2C-SMBus-MS AXI/AHB/APB Controller – System Diagram

The DB-I2C-SMBus-MS-AMBA Controller IP Core targets embedded processor applications with higher performance algorithm requirements or I2C/SMBus transfer requirements to a set of Registers or Memory. While most I2C controllers require high processor interaction involvement, the DB-I2C-SMBus-MS-AMBA contains a parameterized FIFO and Finite State Machine Control for the processor to off-load the I2C/SMBus transfer to the DB-I2C-SMBus-MS-AMBA Controller. Thus, while the DB-I2C-SMBus-MS-AMBA in Master Mode is busy, independently controlling the I2C/SMBus Transmit or Receive transaction of data, or in Slave Mode, allowing the external I2C/SMBus Master device to control the Transmit or Receive of data, the processor can complete other tasks. All Master & Slave Mode Transmit / Receive transfers are with respect to the internal FIFO, thus fully isolating the processor from the I2C/SMBus transfer of a block of data.

Features

- Master / Slave I^2C/SMBus Controller Modes:
  - Master – Transmitter
  - Master – Receiver
  - Slave – Transmitter
  - Slave – Receiver
- Supports three I2C/SMBus bus speeds:
  - Fast Mode Plus (1 Mbit/s)
  - Fast Mode (400 Kb/s)
  - Standard Mode (100 Kb/s)
- I2C compliant features:
  - Multi-Master, Clock Synchronization, Arbitration, SCL held low by Slave, Repeated Start, 7/10-bit addressing, & General Call Addressing
- SMBus compliant features:
  - SMBCLK Clock Low Timeout – User programmable timeout meeting SMBus Time-out requirement
  - SMBDAT minimum data hold time
- Parameterized FIFO memory for off-loading the I^2C/SMBus transfers from the processor:
  - Targets embedded processors with higher performance algorithm requirements, by the I^2C/SMBus Controller independently controlling the Transmit or Receive of bytes of information buffered to and from a FIFO.
- System-level features & integration capabilities:
  - CPU Interface via parameterized FIFO with support for APB / AHB / AXI / AXI-lite / Avalon SoC Interconnect fabrics
  - Enhanced SCL / SDA spike filtering capabilities
  - Enhanced Repeated Start capabilities
- Optional system-level features & integration capabilities:
  - DMA transfer between the I2C/SMBus & Memory (SDRAM / SRAM / FLASH)

  - Direct interface to user Registers within ASIC / ASSP / FPGA device, for Master/Slave transfer across the I2C/SMBus
  - Remote Configuration of a Digital Blocks' I2C/SMBus Slave by an I2C Master
- 13 sources of internal interrupts with masking control
- Compliance with AMBA, I2C, and SMBus specifications:
  - Compliance with AMBA AXI, AHB, APB Protocol Specification (V2.0)
  - Philips/NXP – The I2C-Bus Specification, Version 2.1, January 2000 and UM10204 Rev 6 – 4 April 2014
  - System Management Bus (SMBus) Specification Version 3.0, Dec 2014
- Fully-synchronous, synthesizable Verilog RTL core, with rising-edge clocking, no gated clocks, and no internal tri-states, for easy integration into FPGA or ASIC design flows.

Pin Description

In addition to the AMBA AXI, AHB, or APB Bus interfaces, which include the input CLOCK and RESET signals and the output INTR (interrupt) signal, the I2C/SMBus interface signals are listed in Table 1.

Name	Type	Description
I2C Bus interface		
SDAI	Input	Serial Data
SDAO	Output	Serial Data
SCLI	Input	Serial Clock Line
SCLO	Output	Serial Clock Line

Table 1: DB-I2C-SMBus-MS-AMBA – I/O Pin Description

Verification Method

The DB-I2C-SMBus-MS-AMBA Controller IP Core contains a verification test suite with AMBA AXI, AHB, or APB Bus functional models that program the DB-I2C-SMBus-MS-AMBA control & status registers, generates & sends I2C/SMBus data, monitors the I2C/SMBus protocol, and checks expected results.

The DB-I2C-SMBus-MS-AMBA Controller IP Core has internally been verified as follows:

- Instantiated within an FPGA, controlled by an ARM processor, and communicating with (1) I2C & SMBus Master and I2C & SMBus Slave merchant

semiconductor devices, including devices from NXP & MAXIM; and (2) variety of ASICs containing I2C/SMBus Master & Slave bus interfaces

Customer Evaluation

Digital Blocks offers a variety of methods for prospective customers to evaluate the DB-I2C-SMBus-MS-AMBA. Please contact Digital Blocks for additional information.

Deliverables

The DB-I2C-SMBus-MS-AMBA is available in synthesizable RTL Verilog or a technology-specific netlist for FPGAs, along with Synopsys Design Constraints, a simulation test bench with expected results, datasheet, and user manual.

The DB-I2C-SMBus-MS-AMBA comes along with example C code software for controlling Transmit and Receive Transactions in an Eclipse-based ARM Integrated Development Environment (IDE).

Ordering Information

Please contact Digital Blocks for additional technical, pricing, evaluation, and support information.

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