Digital Blocks
Semiconductor IP

DB-I2C-SMBUS-MS-AXI
DB-I2C-SMBUS-MS-AHB
DB-I2C-SMBUS-MS-APB
AMBA Bus I2C-SMBus Controller

General Description

The Digital Blocks DB-I2C-SMBus-MS-AMBA Controller IP Core is an I2C/SMBus Master/Slave Controller, interfacing a microprocessor via the AMBA AXI, AHB, or APB Bus to an I2C/SMBus Interconnect. Both I2C and SMBus protocols are supported.

The System Management Bus (SMBus) is a two-wire bidirectional interface standard (SCL is Clock, SDA is Data) for transfer of bytes of information between two or more compliant SMBus devices, typically with a microprocessor behind the master controller and one or more slave devices.

The DB-I2C-SMBus-MS-AMBA is a Master/Slave SMBus Controller that in Master Mode controls the Transmit or Receive of data to or from slave SMBus devices while in Slave Mode allows an external SMBus Master device to control the Transmit or Receive of data.

In an ASIC / ASSP / FPGA integrated circuit, typically, the microprocessor is an ARM or RISC-V processor, but can be any embedded processor. Figure 1 depicts the system view of the DB-I2C-SMBus-MS-AMBA Controller IP Core embedded within an integrated circuit device with its Microprocessor Configuration.

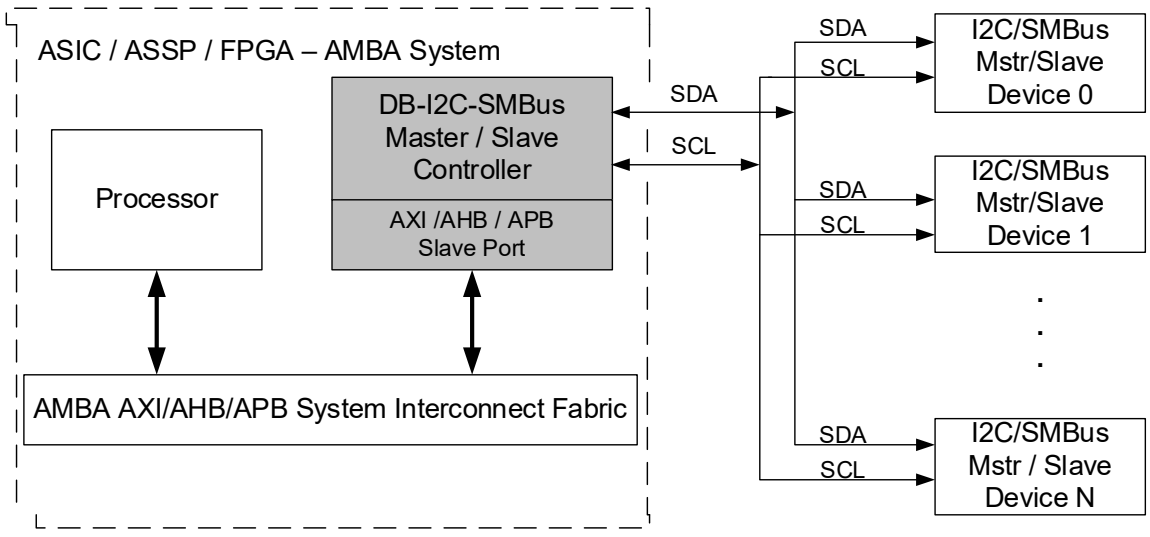

Figure 1: DB-I2C-SMBus-MS AXI/AHB/APB Controller – System Diagram

Features

- SMBus compliant features:
  - SMBCLK Clock Low Timeout – User programmable timeout meeting SMBus Time-out requirement
  - SMBDAT minimum data hold time
  - SMBus Address Resolution Protocol
- Master / Slave SMBus Controller Modes:
  - Master – Transmitter, Master – Receiver,
  - Slave – Transmitter, Slave – Receiver
- Supports unique SMBus bus speeds:
  - 10 KHz to 100 KHz
- For I2C use, Supports three or four I2C bus speeds:
  - Standard Mode (100 Kb/s)
  - Fast Mode (400 Kb/s)
  - Fast Mode Plus (1 Mbit/s)
  - Hs-mode (3.4 Mb/s) (optional licensing feature)
- SMBus/I2C compliant features:
  - Multi-Master, Clock Synchronization, Arbitration, SCL held low by Slave, Repeated Start, 7/10-bit addressing, & General Call Addressing
- Parameterized FIFO memory and FSM control for off-loading the SMBus transfers from the processor.
- System-level features & integration capabilities:
  - CPU Interface via parameterized FIFO with support for APB / AHB / AXI / AXI-lite / Avalon SoC Interconnect fabrics
  - Enhanced SCL / SDA spike filtering capabilities
  - Enhanced Repeated Start capabilities
- Optional system-level features & integration capabilities:
  - DMA transfer between the SMBus & Memory (SDRAM / SRAM / FLASH)
  - Direct interface to user Registers within ASIC / ASSP / FPGA device, for Master/Slave transfer across the SMBus
- 13 sources of internal interrupts with masking control
- Compliance with AMBA, I2C, and SMBus specifications:
  - Compliance with AMBA AXI, AHB, APB Protocol Specification (V2.0)
  - Philips/NXP – The I2C-Bus Specification, Version 2.1, January 2000 and UM10204 Rev 7.0 – 1 October 2021
  - System Management Bus (SMBus) Specification Version 3.1, March 2018
- Fully-synchronous, synthesizable Verilog RTL core, with rising-edge clocking, no gated clocks, and no internal tri-states, for easy integration into FPGA or ASIC design flows.

Verification Method

The DB-I2C-SMBus-MS-AMBA Controller IP Core contains a verification test suite with AMBA AXI, AHB, or APB Bus functional models that program the DB-I2C-SMBus-MS-AMBA control & status registers, generates & sends SMBus and I2C data, monitors the SMBus and I2C protocol, and checks expected results.

Customer Evaluation

Digital Blocks offers a variety of methods for prospective customers to evaluate the DB-I2C-SMBus-MS-AMBA. Please contact Digital Blocks for additional information.

Deliverables

The DB-I2C-SMBus-MS-AMBA is available in synthesizable RTL Verilog or a technology-specific netlist for FPGAs, along with Synopsys Design Constraints, a simulation test bench with expected results, datasheet, and user manual.

Ordering Information

Please contact Digital Blocks for additional technical, pricing, evaluation, and support information.

Digital Blocks, Inc.
PO Box 192
587 Rock Rd
Glen Rock, NJ 07452 USA
Phone: +1-201-251-1281
eFax: +1-702-552-1905
info@digitalblocks.com