General Description

The DB-I2C-S-AHB-BRIDGE is an I^2C Slave Controller IP Core focused on low VLSI footprint ASIC / ASSP designs not requiring internal configuration & control registers (and thus no local host CPU required), and an AHB Master interface for read/write to the user system. The DB-I2C-S-AHB-BRIDGE processes the I^2C protocol & physical layers, and receives & transmits bytes with respect to the I^2C payload via a bridge AHB Master Interface to user registers or memory.

The DB-I2C-S-AHB-BRIDGE runs off the AHB Master external clock input within the ASIC / ASSP, providing a synchronous design while offering I^2C spike filtering of SDA and SCL.

The DB-I2C-S-AHB-BRIDGE is a member of Digital Blocks DB-I2C Controller IP Core family, which includes I^2C Master/Slave, I^2C Master-only, and I^2C Slave-only configurations.

Figure 1 depicts the DB-I2C-S-AHB-BRIDGE Core system view. The IP is configured by internal pre-synthesis parameters and post-synthesis top-level input signals, receives input clock and reset, and performs I^2C Slave-Receiver transfers (for writing data to the AHB via its AHB Master Interface) and Slave-Transmitter transfers (for reading data from the AHB via the AHB Master Interface).

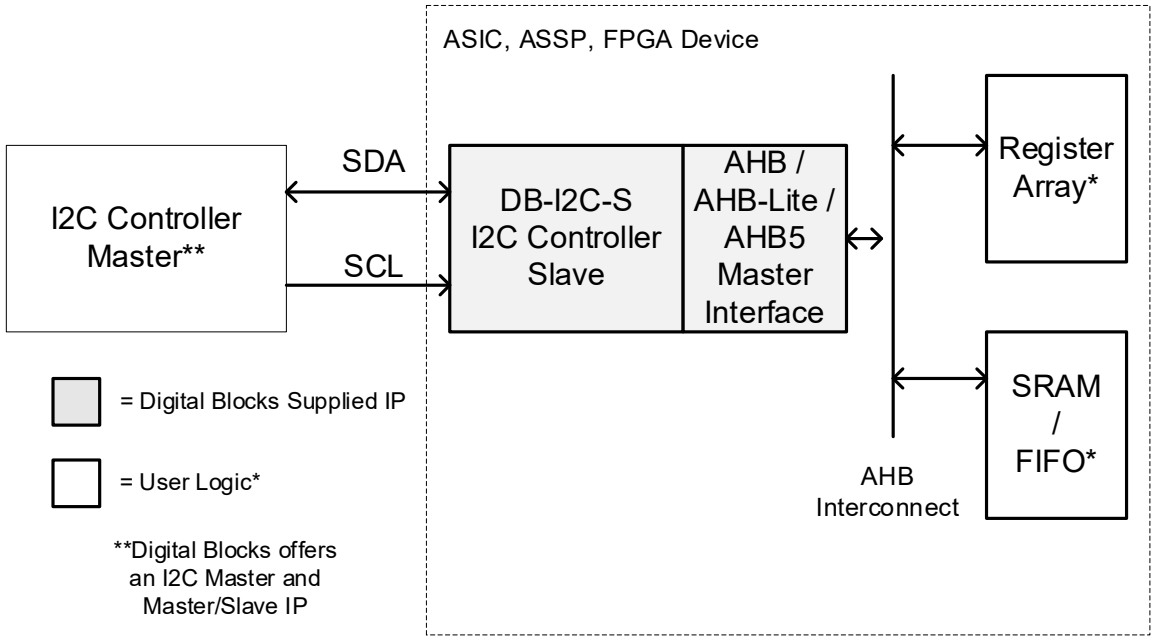

Figure 1: DB-I2C-S-AHB-BRIDGE Controller - System View

Features

- I2C Slave Controller - Implements Slave-only protocol for smaller VLSI footprint, for applications requiring Slave–Receiver and Slave–Transmitter capability
- AHB Master Interface – bridging the I^2C Bus to the AHB Bus
  - AHB5, AHB 2.0, AHB-Lite releases
- Autonomous I2C Slave Controller:
  - No local CPU host required
  - No configuring of control/status registers
- Slave I^2C Controller Modes:
  - Slave – Transmitter
  - Slave – Receiver
- Supports five I2C bus speeds:
  - Standard Mode (100 Kb/s)
  - Fast Mode (400 Kb/s)
  - Fast Mode plus (1 Mbit/s)
  - Ultra fast mode (5 Mbit/s)
  - Hs-mode (3.4 Mbit/s)
- 7- or 10-bit I2C Slave ID addressing, SCL Low Wait States
- Digital filter for the received SDA and SCL lines
- Compliance with I2C specifications:
  - Philips – The I2C-Bus Specification, Version 2.1, January 2000
  - NXP Rev 7.0 October 1, 2021
- Fully-synchronous, synthesizable Verilog RTL core, with rising-edge clocking, no gated clocks, and no internal tri-states, for easy integration into FPGA or ASIC design flows.

Pin Description

The DB-I2C-S-AHB-BRIDGE I2C Slave Controller interface signals are listed in Table 1

Name	Type	Description
I2C Bus Interface		
SDAI	Input	Serial Data
SDAO	Output	Serial Data
SCLI	Input	Serial Clock Line
AHB Master Interface		
See AMBA AHB Protocol Specification, 2021 See AMBA 5 AHB Protocol Specification, AHB5, AHB-Lite, 2015		

Table 1: DB-I2C-S-AHB-BRIDGE – I/O Pin Description

Verification Method

The DB-I2C-S-AHB-BRIDGE Controller IP Core contains a test suite that generates & sends I2C transactions, monitors the I2C bus protocol, and checks expected results.

Customer Evaluation

Digital Blocks offers a variety of methods for prospective customers to evaluate the DB-I2C-S-AHB-BRIDGE. Please contact Digital Blocks for additional information.

Deliverables

The DB-I2C-S-AHB-BRIDGE is available in synthesizable RTL Verilog or a technology-specific netlist for FPGAs, along with Synopsys Design Constraints, a simulation test bench with expected results, datasheet, and user manual.

Ordering Information

Please contact Digital Blocks for additional technical, pricing, evaluation, and support information.

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