

General Description

The Digital Blocks DB-I2C-S-APB Controller IP Core interfaces an ARM, MIPS, PowerPC, ARC or other high performance microprocessor via the AMBA 2.0 APB System Interconnect Fabric to an I2C Bus. The I2C is a two-wire bidirectional interface standard (SCL is Clock, SDA is Data) for transfer of bytes of information between two or more compliant I2C devices.

The DB-I2C-S-APB is a Slave I2C Controller that controls the Transmit or Receive of data to or from external Master I2C devices. Figure 1 depicts the system view of the DB-I2C-S-APB Controller IP Core embedded within an integrated circuit device.

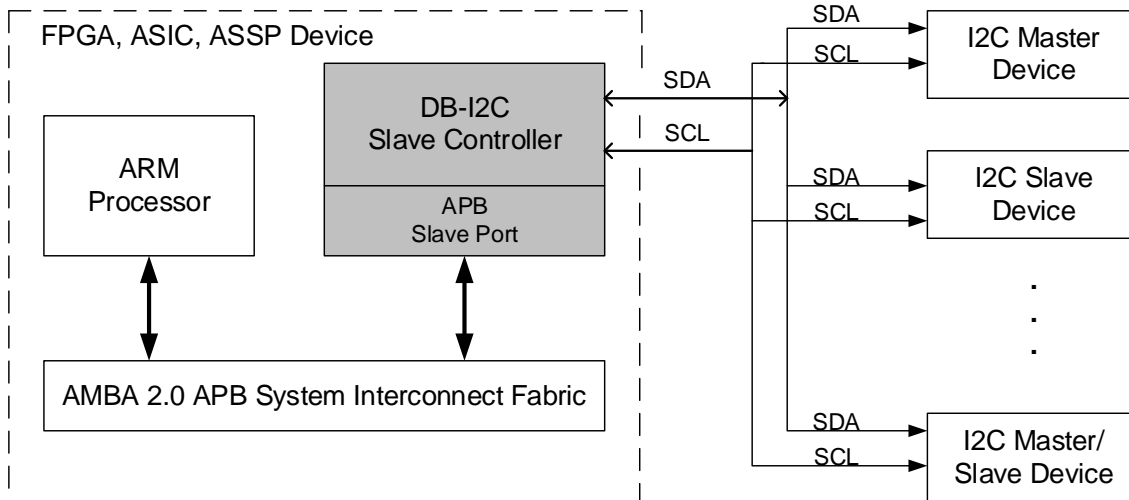


Figure 1: DB-I2C-S-APB Controller – System Diagram

The DB-I2C-S-APB Controller IP Core targets embedded processor applications with higher performance algorithm requirements. While most I2C controllers require high processor interaction involvement, the DB-I2C-S-APB contains a parameterized FIFO and Finite State Machine control for the processor to off-load the I2C transfer to the DB-I2C-M-APB Controller. Thus, while the DB-I2C-S-APB is busy, independently controlling the I2C Transmit or Receive transaction of data, the processor can go off and complete other tasks. Note that the Slave only capability of the DB-I2C-S-APB adds to its small VLSI footprint requirements.

The DB-I2C-S-APB could be paired with the DB-I2C-M-APB or DB-I2C-MS-APB in another ASIC/ASSP/FPGA, for robust & VLSI efficient transfer of blocks of data.

Features

- Slave I²C Controller Modes:
 - Slave – Transmitter
 - Slave – Receiver
- Supports four I2C bus speeds:
 - Hs-Mode (3.4+ Mb/s)
 - Fast Mode Plus (1 Mbit/s)
 - Fast Mode (400 Kb/s)
 - Standard Mode (100 Kb/s)
 - Ultra Fast-mode (5 Mbit/s)
- Parameterized FIFO memory for off-loading the I²C transfers from the processor:
 - Targets embedded processors with higher performance algorithm requirements, by the I²C Controller independently controlling the Transmit or Receive of bytes of information buffered to and from a FIFO.
- I2C compliant features:
 - Repeated Start, 7/10-bit addressing, General Call Addressing, & SCL Low Wait States
- Enhanced system-level features & integration capabilities:
 - CPU Interface via parameterized FIFO with support for APB / AHB / AXI / AXI-lite / Avalon interconnect fabrics
 - Enhanced SCL / SDA spike filtering capabilities
 - Enhanced Repeated Start capabilities
- Enhanced system-level features & integration capabilities (OPTIONAL):
 - DMA transfer between the I2C Bus & Memory (SDRAM / SRAM / FLASH)
 - Direct interface to user Registers within ASIC / ASSP / FPGA device, for Master/Slave transfer across the I2C Bus
 - Remote Configuration of a Digital Blocks' I2C Slave by an I2C Master
- 8 sources of internal interrupts with masking control
- Compliance with AMBA 2.0 and I2C specifications:
 - AMBA Specification (Rev 2.0), APB Bus
 - Philips/NXP – The I2C-Bus Specification, Version 2.1, January 2000 and UM10204 Rev 6 – 4 April 2014
- Fully-synchronous, synthesizable Verilog RTL core, with rising-edge clocking, no gated clocks, and no internal tri-states, for easy integration into FPGA or ASIC design flows.

Digital Blocks offers I2C Master/Slave, Master-only, and Slave-only Controller IP supporting Hs-Mode / Fast Mode Plus / Fast Mode / Standard Mode.

Pin Description

The DB-I2C-S-APB I2C Slave Controller interface signals are listed in Table 1.

| Name | Type | Description |
|--------------------------|-------------|-------------------------------------|
| APB Bus Interface | | |
| PCLK | Input | Bus Clock |
| PRESETn | Input | APB Reset (Active Low) |
| PADDR[11:0] | Input | APB Address Bus |
| PSEL_DB_I2C | Input | APB Select for DB-I2C |
| PENABLE | Input | APB Strobe |
| PWRITE | Input | APB Transfer Direction (Read/Write) |
| PRDATA[31:0] | Output | APB Read Data Bus |
| PWDATA[31:0] | Input | APB WriteData Bus |
| I2C Bus interface | | |
| SDAi | Input | Serial Data |
| SDAo | Output | Serial Data |
| SCLi | Input | Serial Clock Line |

Table 1: DB-I2C-S-APB – I/O Pin Description

Verification Method

The DB-I2C-S-APB Controller IP Core contains a test suite that generates & sends I2C transactions, monitors the I2C bus protocol, and checks expected results.

The DB-I2C-S-APB Controller IP Core has internally been verified as follows:

- Instantiated within an FPGA, and communicating with NXP I2C Master IP Controller, and A ARM processor for expected data checking. I2C Bus Compliance testing with lab instrumentation.
- Instantiated within an FPGA, and communicating with Digital Blocks I2C Master IP Controller, and A NIOS II processor for expected data checking.
- Internal projects interfacing to NXP, Atmel I2C Masters.
- Customer FPGA / ASIC implementations.

Customer Evaluation

Digital Blocks offers a variety of methods for prospective customers to evaluate the DB-I2C-S-APB. Please contact Digital Blocks for additional information.

Deliverables

The DB-I2C-S-APB is available in synthesizable RTL Verilog or a technology-specific netlist for FPGAs, along with Synopsys Design Constraints, a simulation test bench with expected results, datasheet, and user manual.

Ordering Information

Please contact Digital Blocks for additional technical, pricing, evaluation, and support information.

Digital Blocks, Inc.
PO Box 192
587 Rock Rd
Glen Rock, NJ 07452 USA
Phone: +1-201-251-1281
eFax: +1-702-552-1905
info@digitalblocks.com

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