General Description

The Digital Blocks DB-I2C-S-Hs-Mode I2C Slave Controller IP Core interfaces user Registers to an I2C Bus or Memory (SDRAM / SRAM / Flash / FIFO) or any Peripheral or CPU connecting through an internal AHB / APB / AXI / Avalon / Qsys Bus to an I2C Bus in Hs-Mode (3.4 Mbit/s) / Fast-Mode Plus (1 Mbit/s) / Fast-Mode (400 Kbit/s) / Standard-Mode (100 Kbit/s).

The DB-I2C-S-Hs-Mode Controller implements the Slave-Transmit and Slave-Receive protocol according to the Philips I2C-Bus Specification, Version 2.1 as well as the updated NXP Rev .5 October 9, 2012 Specification.

Figure 1 depicts the system view of the DB-I2C-S-Hs-Mode Slave Controller IP Core embedded within an ASIC, ASSP or FPGA device. The DB-I2C-S-Hs-Mode Controller receives and transmits data with respect to an external I2C Master Controller. The DB-I2C-S-Hs-Mode can interface to a user Register Array, Memory such as SRAM, SDRAM, Flash, or a FIFO, or a Peripheral or CPU.

The DB-I2C-S-Hs-Mode IP Core can function standalone, without the requirement for an embedded processor.
Features

- I2C Slave Controller - Implements Slave-only protocol for smaller VLSI footprint:
  - Slave–Transmitter
  - Slave–Receiver
- Supports four I2C bus speeds:
  - Hs-Mode (3.4+ Mb/s)
  - Fast Mode Plus (1 Mbit/s)
  - Fast Mode (400 Kb/s)
  - Standard Mode (100 Kb/s)
- Digital Blocks optionally supplies a RTL Parameterized Register Array the user can use to construct their registers, or a Register Array / SDRAM / SRAM / Flash / FIFO Interface the user can use to connect to their existing designs, or an AHB / APB / AXI / Avalon Master interface the user can connect Memory or Peripherals to that are participating in the I2C transfer.
- DB-I2C-S-Hs-Mode Controller supports single register / memory access or burst access with address auto-increment capability.
- 7- or 10-bit addressing, General Call, SCL Low Wait States
- Enhanced SCL / SDA spike filtering capabilities
- 13 sources of internal interrupts with masking control
- Compliance with I2C specifications:
  - Compliance with AMBA AXI / AHB/ APB Protocol Specifications
  - Compliance with Avalon / Qsys Protocol Specifications
  - NXP Rev .5 October 9, 2012
- Fully-synchronous, synthesizable Verilog RTL core, with rising-edge clocking, no gated clocks, and no internal tri-states, for easy integration into FPGA or ASIC design flows.

Digital Blocks offers I2C Master/Slave, Master-only, and Slave-only Controller IP supporting Hs-Mode / Fast Mode Plus / Fast Mode / Standard Mode.
Pin Description

The DB-I2C-S-Hs-Mode I2C Slave Controller interface signals are listed in Table 1.

<table>
<thead>
<tr>
<th>Name</th>
<th>Type</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td><strong>I2C Bus Interface</strong></td>
</tr>
<tr>
<td>SDAI</td>
<td>Input</td>
<td>Serial Data</td>
</tr>
<tr>
<td>SDAO</td>
<td>Output</td>
<td>Serial Data</td>
</tr>
<tr>
<td>SCLI</td>
<td>Input</td>
<td>Serial Clock Line</td>
</tr>
</tbody>
</table>

|      |       | **Register Array / SRAM / FIFO / AMBA / Avalon Interface** |
|      |       | Please contact Digital Blocks for more information |

Table 1: DB-I2C-S-Hs-Mode – I/O Pin Description
Verification Method

The DB-I2C-S-Hs-Mode Controller IP Core contains a test suite that generates & sends I2C transactions, monitors the I2C bus protocol, and checks expected results.

The DB-I2C-S-Hs-Mode Controller IP Core has internally been verified as follows:
- Instantiated within an FPGA, and communicating with NXP I2C Master IP Controller, and an ARM processor within the FPGA for expected data checking.
- I2C Bus Compliance testing with lab instrumentation.
- Customer Implementations.

Customer Evaluation

Digital Blocks offers a variety of methods for prospective customers to evaluate the DB-I2C-S-Hs-Mode. Please contact Digital Blocks for additional information.

Deliverables

The DB-I2C-S-Hs-Mode is available in synthesizable RTL Verilog or a technology-specific netlist for FPGAs, along with Synopsys Design Constraints, a simulation test bench with expected results, datasheet, and user manual.

Ordering Information

Please contact Digital Blocks for additional technical, pricing, evaluation, and support information.

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