

General Description

The DB-I2C-S-REG is an I²C Slave Controller IP Core focused on low VLSI footprint ASIC / ASSP designs not requiring internal configuration & control registers (and thus no local host CPU required). The DB-I2C-S-REG processes the I²C protocol & physical layers, and receives & transmits bytes with respect to the I²C payload to / from User Registers or SRAM/FIFO.

The DB-I2C-S-REG runs off an external clock input within the ASIC / ASSP, providing a synchronous design while offering I²C spike filtering of SDA and SCL.

The DB-I2C-S-REG is a member of Digital Blocks DB-I2C Controller IP Core family, which includes I²C Master/Slave, I²C Master-only, and I²C Slave-only configurations.

Figure 1 depicts the DB-I2C-S-REG Core system view. The IP is configured by internal pre-synthesis parameters and post-synthesis top-level input signals, receives input clock and reset, and performs I²C Slave-Receiver transfers (for loading User Registers) and Slave-Transmitter transfers (for reading User Registers).

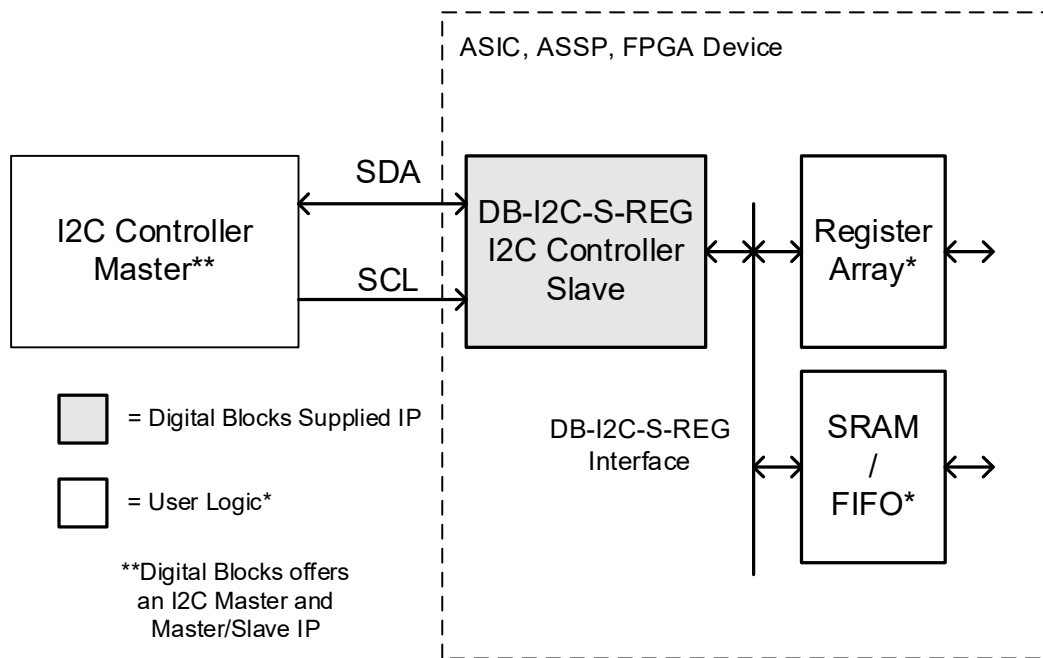


Figure 1: DB-I2C-S-REG Controller with Register I/F – System Diagram

Features

- I2C Slave Controller - Implements Slave-only protocol for smaller VLSI footprint, for applications requiring Slave–Receiver and Slave–Transmitter capability
- Autonomous I2C Slave Controller:
 - No local CPU host required
 - No configuring of control/status registers
- DB-I2C-S-REG Controller supports single register/memory access with address auto-increment capability
 - 8/16-bit User Address Register Space
- Slave I²C Controller Modes:
 - Slave – Transmitter
 - Slave – Receiver
- Supports five I2C bus speeds:
 - Standard Mode (100 Kb/s)
 - Fast Mode (400 Kb/s)
 - Fast Mode plus (1 Mbit/s)
 - Ultra fast mode (5 Mbit/s)
 - Hs-mode (3.4 Mbit/s)
- 7- or 10-bit I2C Slave ID addressing, SCL Low Wait States
- Digital filter for the received SDA and SCL lines
- Compliance with I2C specifications:
 - Philips – The I2C-Bus Specification, Version 2.1, January 2000
 - NXP Rev 7 – 1 Oct 2021
- Fully-synchronous, synthesizable Verilog RTL core, with rising-edge clocking, no gated clocks, and no internal tri-states, for easy integration into FPGA or ASIC design flows.

Pin Description

The DB-I2C-S-REG I2C Slave Controller interface signals are listed in Table 1.

Name	Type	Description
I2C Bus Interface		
SDAI	Input	Serial Data
SDAO	Output	Serial Data
SCLI	Input	Serial Clock Line
Global Reset, Clock		

RESETN	Input	Power-up Reset
CLK	Input	Clock
DB-I2C-S-REG Interface of User Registers		
Please contact Digital Blocks for more information		

Table 1: DB-I2C-S-REG – I/O Pin Description

Verification Method

The DB-I2C-S-REG Controller IP Core contains a test suite that generates & sends I2C transactions, monitors the I2C bus protocol, and checks expected results.

Customer Evaluation

Digital Blocks offers a variety of methods for prospective customers to evaluate the DB-I2C-S-REG. Please contact Digital Blocks for additional information.

Deliverables

The DB-I2C-S-REG is available in synthesizable RTL Verilog or a technology-specific netlist for FPGAs, along with Synopsys Design Constraints, a simulation test bench with expected results, datasheet, and user manual.

Ordering Information

Please contact Digital Blocks for additional technical, pricing, evaluation, and support information.

Digital Blocks, Inc.
PO Box 192
587 Rock Rd
Glen Rock, NJ 07452 USA
Phone: +1-201-251-1281
eFax: +1-702-552-1905
info@digitalblocks.com

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