

General Description

The Digital Blocks DB-I2C-S-SCL-CLK-APB Controller IP Core interfaces an ARM, MIPS, PowerPC, ARC or other high-performance microprocessor via the AMBA 2.0 APB System Interconnect Fabric to an I2C Bus. The I2C is a two-wire bidirectional interface standard (SCL is Clock, SDA is Data) for transfer of bytes of information between two or more compliant I2C devices.

The DB-I2C-S-SCL-CLK-APB, in the I2C Slave Controller Core managing the I2C protocol & physical layer, contains no free running clock, while interfacing through dual-clock FIFOs to the AMBA APB Bus, for a low power, low noise Microprocessor interface to the I2C Bus. The I2C Slave Controller Core runs off the external SCL clock while the APB side off the APB Clock.

The DB-I2C-S-SCL-CLK-APB Controller implements the Slave-Transmit and Slave-Receive protocol according to the Philips I2C-Bus Specification, Version 2.1 as well as the updated NXP UM10204 Rev 7 – 1 Oct 2021 Specification.

The DB-I2C-S-SCL-CLK-APB is a member of Digital Blocks DB-I2C Controller IP Core family, which includes I²C Master/Slave, I²C Master-only, and I²C Slave-only configurations.

Figure 1 depicts the system view of the DB-I2C-S-SCL-CLK-APB Controller IP Core embedded within an ASIC, ASSP or FPGA device.

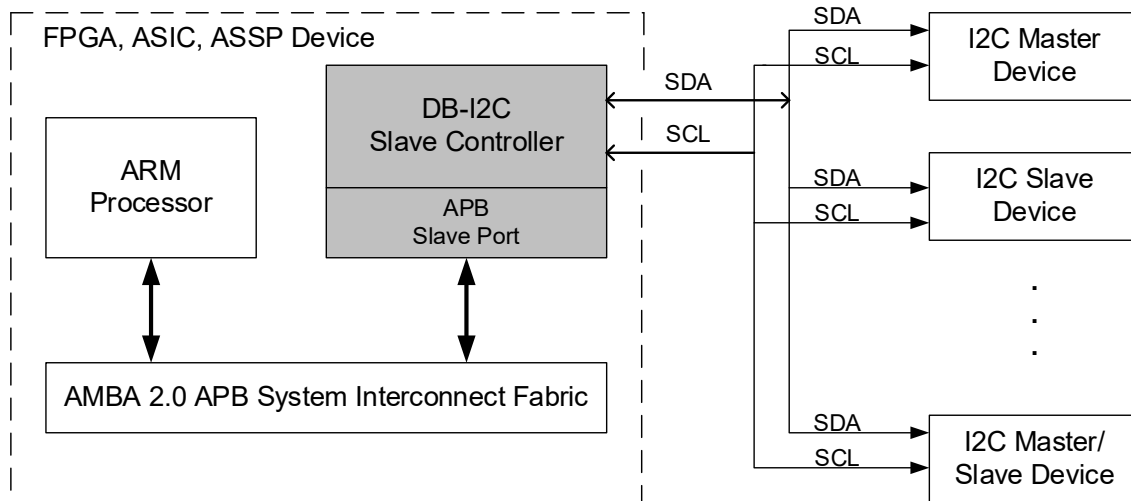


Figure 1: DB-I2C-S-SCL-CLK-APB Controller – System Diagram

Features

- Slave I²C Controller Modes:
 - Slave – Transmitter
 - Slave – Receiver
- Supports four I2C bus speeds:
 - Hs-Mode (3.4+ Mb/s)
 - Fast Mode Plus (1 Mbit/s)
 - Fast Mode (400 Kb/s)
 - Standard Mode (100 Kb/s)
- Low power, low noise applications requiring non-free running SCL Clock in the I2C protocol & physical layer logic processing and APB Clock only to interface to the Microprocessor.
- Parameterized FIFO memory for off-loading the I²C transfers from the processor:
 - Targets embedded processors with higher performance algorithm requirements, by the I²C Controller independently controlling the Transmit or Receive of bytes of information buffered to and from a FIFO.
- I2C compliant features:
 - Repeated Start, 7/10-bit addressing
- Enhanced system-level features & integration capabilities:
 - CPU Interface via parameterized FIFO with support for APB / AHB / AXI / AXI-lite / Avalon interconnect fabrics
- Enhanced system-level features & integration capabilities (OPTIONAL):
 - Direct interface to user Registers within ASIC / ASSP / FPGA device, for Master/Slave transfer across the I2C Bus
- 5 sources of internal interrupts with masking control
- Compliance with AMBA 2.0 and I2C specifications:
 - AMBA Specification (Rev 2.0), APB Bus
 - Philips/NXP – The I2C-Bus Specification, Version 2.1, January 2000 and UM10204 Rev 7 – 1 Oct 2021

Digital Blocks offers I2C Master/Slave, Master-only, and Slave-only Controller IP supporting Hs-Mode / Fast Mode Plus / Fast Mode / Standard Mode.

Pin Description

The DB-I2C-S-SCL-CLK-APB I2C Slave Controller interface signals are listed in Table 1. Note that a bi-directional driver is available for SDAI / SDAO.

Name	Type	Description
APB Bus Interface		
PCLK	Input	Bus Clock
PRESETn	Input	APB Reset (Active Low)
PADDR[11:0]	Input	APB Address Bus
PSEL DB I2C	Input	APB Select for DB-I2C
PENABLE	Input	APB Strobe
PWRITE	Input	APB Transfer Direction (Read/Write)
PRDATA[31:0]	Output	APB Read Data Bus
PWDATA[31:0]	Input	APB WriteData Bus
I2C Bus interface		
SDAi	Input	Serial Data
SDAo	Output	Serial Data
SCLi	Input	Serial Clock Line

Table 1: DB-I2C-S-SCL-CLK-APB – I/O Pin Description

Verification Method

The DB-I2C-S-SCL-CLK-APB Controller IP Core contains a test suite that generates & sends I2C transactions, monitors the I2C bus protocol, and checks expected results.

The DB-I2C-S-SCL-CLK-APB Controller IP Core has internally been verified as follows:

- Instantiated within a customer's series of FPGA for verification and ASICs for production.

Customer Evaluation

Digital Blocks offers a variety of methods for prospective customers to evaluate the DB-I2C-S-SCL-CLK-APB. Please contact Digital Blocks for additional information.

Deliverables

The DB-I2C-S-SCL-CLK-APB is available in synthesizable RTL Verilog or a technology-specific netlist for FPGAs, along with Synopsys Design Constraints, a simulation test bench with expected results, datasheet, and user manual.

Ordering Information

Please contact Digital Blocks for additional technical, pricing, evaluation, and support information.

Digital Blocks, Inc.
PO Box 192
587 Rock Rd
Glen Rock, NJ 07452 USA
Phone: +1-201-251-1281
eFax: +1-702-552-1905
info@digitalblocks.com

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