General Description

The DB-I2C-S-SCL-CLK is an \(^2\text{C}\) Slave Controller IP Core focused on low power, low noise ASIC / ASSP designs requiring the configuration & control of registers with no free running clock. The DB-I2C-S-SCL-CLK processes the \(^2\text{C}\) protocol & physical layers, and receives & transmits bytes with respect to the \(^2\text{C}\) payload to / from User Registers within an ASIC / ASSP / FPGA device. The DB-I2C-S-SCL-CLK Controller implements the Slave-Transmit and Slave-Receive protocol according to the Philips \(^2\text{C}\)-Bus Specification, Version 2.1 as well as the updated NXP Rev .5 October 9, 2012 Specification.

The DB-I2C-S-SCL-CLK is a member of Digital Blocks DB-I2C Controller IP Core family, which includes \(^2\text{C}\) Master/Slave, \(^2\text{C}\) Master-only, and \(^2\text{C}\) Slave-only configurations.

Figure 1 depicts the system view of the DB-I2C-S-SCL-CLK Controller IP Core embedded within an ASIC, ASSP or FPGA device. The DB-I2C-S-SCL-CLK Controller receives and transmits data with respect to an external \(^2\text{C}\) Master Controller. The DB-I2C-S-SCL-CLK internally interfaces to User Registers.

![Figure 1: DB-I2C-S-SCL-CLK Controller - System View](image-url)
**Features**

- **I2C Slave Controller** - Implements Slave-only protocol for smaller VLSI footprint, for applications requiring Slave–Receiver and Slave–Transmitter capability
- **SCL Clock** only for low power, low noise applications requiring configuration & management of User Registers
- **7- or 10-bit addressing**; **General Call, SCL Low Wait States**
- **Supports five I²C bus speeds:**
  - Standard mode (100 Kb/s)
  - Fast mode (400 Kb/s)
  - Fast mode plus (1 Mbit/s)
  - Ultra fast mode (5 Mbit/s)
  - Hs-mode (3.4 Mbit/s)
- **Compliance with I2C specifications:**
  - NXP Rev .5 October 9, 2012
- **Fully-synchronous, synthesizable Verilog RTL core. Easy integration into FPGA or ASIC design flows.**

**Pin Description**

The DB-I2C-S-SCL-CLK I2C Slave Controller interface signals are listed in Table 1. Note that a bi-directional driver is available for SDAI / SDAO.

<table>
<thead>
<tr>
<th>Name</th>
<th>Type</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td><strong>I2C Bus Interface</strong></td>
<td></td>
</tr>
<tr>
<td>SDAI</td>
<td>Input</td>
<td>Serial Data</td>
</tr>
<tr>
<td>SDAO</td>
<td>Output</td>
<td>Serial Data</td>
</tr>
<tr>
<td>SCLI</td>
<td>Input</td>
<td>Serial Clock Line</td>
</tr>
<tr>
<td></td>
<td><strong>User Register Interface</strong></td>
<td></td>
</tr>
</tbody>
</table>

Please contact Digital Blocks for more information

*Table 1: DB-I2C-S-SCL-CLK – I/O Pin Description*
Verification Method

The DB-I2C-S-SCL-CLK Controller IP Core contains a test suite that generates & sends I2C transactions, monitors the I2C bus protocol, and checks expected results.

The DB-I2C-S-SCL-CLK Controller IP Core has internally been verified as follows:
- Instantiated within an FPGA, and communicating with NXP I2C Master IP Controller.
- Instantiated within an FPGA, and communicating with Digital Blocks I2C Master IP Controller, and a NIOS II processor for expected data checking.
- Customer Implementations

Customer Evaluation

Digital Blocks offers a variety of methods for prospective customers to evaluate the DB-I2C-S-SCL-CLK. Please contact Digital Blocks for additional information.

Deliverables

The DB-I2C-S-SCL-CLK is available in synthesizable RTL Verilog or a technology-specific netlist for FPGAs, along with Synopsys Design Constraints, a simulation test bench with expected results, datasheet, and user manual.

Ordering Information

Please contact Digital Blocks for additional technical, pricing, evaluation, and support information.

Digital Blocks, Inc.
PO Box 192
587 Rock Rd
Glen Rock, NJ 07452 USA
Phone: +1-201-251-1281
eFax: +1-702-552-1905
info@digitalblocks.com

Copyright © Digital Blocks, Inc. 2007 - 2018, ALL RIGHTS RESERVED

###
Digital Blocks is a registered trademark of Digital Blocks, Inc.
All other trademarks are the property of their respective owners