General Description

The Digital Blocks DB-I3C-BASIC-MS-APB IP Core connects an embedded processor on the AMBA APB bus to an I3C bus, compliant with the MIPI I3C Basic v1.2 specification. I3C is a two-wire bus (SCL clock, SDA data) that carries I3C devices and legacy I2C devices together, and is the upgrade path from I2C.

The core implements both I3C roles – Controller and Target – selected at run time, and passes the Controller role between devices as a Secondary Controller. It supports SDR, the HDR-DDR and HDR-BT high data rate modes including HDR-BT Multi-Lane, and legacy I2C. At 12.5 MHz SCL it reaches 12.5 Mbps in SDR, 25 Mbps in HDR-DDR and HDR-BT, and 50 / 100 Mbps in HDR-BT Multi-Lane x2 / x4.

Figure 1 shows the core in an ASIC, ASSP or FPGA with an embedded processor, typically ARM or RISC-V.

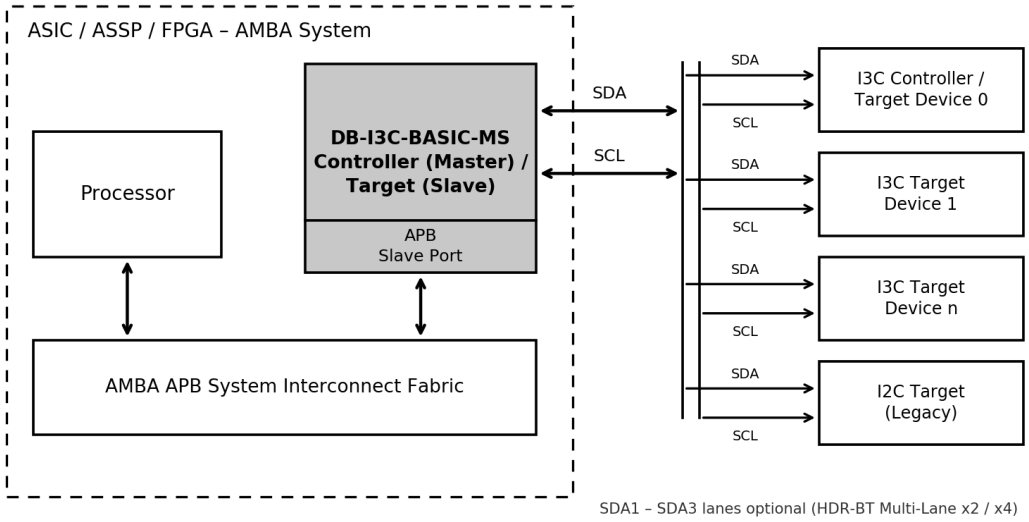

Figure 1: DB-I3C-BASIC-MS-APB Controller / Target System Diagram

Features

- Dual-role MIPI I3C Basic v1.2 Controller / Target, role selected at run time; Controller-only (DB-I3C-BASIC-M-APB) and Target-only (DB-I3C-BASIC-S-APB) configurations for a smaller footprint
- Bus modes and data rates at 12.5 MHz SCL:
  - SDR – 12.5 Mbps; legacy I2C devices on the same bus
  - HDR-DDR – 25 Mbps

  - HDR-BT – 25 Mbps; Multi-Lane x2 / x4 – 50 / 100 Mbps (build option)

- Transfers:

  - Private read / write, broadcast and direct CCCs; whole frames run from the FIFO in hardware, START to STOP
  - CCCs in HDR-DDR and HDR-BT, with flow control and early termination
  - Controller clock stalling – the bus waits instead of aborting when the FIFO runs empty or full

- Bus configuration and management:

  - Dynamic address assignment (ENTDAA) and static-address assignment (SETDASA, SETAASA); Target static address and I2C mode before a dynamic address is assigned
  - Controller device table, 16 devices by default (parameterized)
  - Group addressing
  - In-Band Interrupts with payload, Pending Read notification, Hot-Join
  - Target Reset with reset actions; Activity States
  - Device capability reporting: BCR, DCR, PID, GETCAPS, GETSTATUS, GETMXDS

- Secondary Controller (Basic optional feature) – build option:

  - Controller role hand-off in both directions: Controller Role Request, role offer and acceptance, and publication of the device and group tables to the new Controller
  - Pull-up and keeper control outputs for a glitch-free hand-off; recovery when the new Controller fails to take the bus; Dead Bus Recovery

- Error detection and recovery:

  - All Basic v1.2 Target and Controller error types, with recovery
  - Bus-recovery engine: stuck-SDA recovery, forced STOP, HDR Exit
  - HDR parity and CRC checks with per-message status and error counters

- Timing Control, Asynchronous Mode 0 – build option: Target In-Band Interrupts carry a time stamp from an always-on time-stamp clock
- Specification version: I3C Basic v1.2 by default, with I3C Basic v1.1.1 behavior selectable by register – bus-wide or per Target – for mixed-version buses, from one netlist
- Separate TX and RX FIFOs, parameterized (256 bytes by default)
- Integration:

  - APB, or AXI4-Lite from the same RTL; AHB and AXI on request
  - Single interrupt with per-source mask and status
  - Build options: HDR modes, Multi-Lane x1 / x2 / x4, Secondary Controller, Async Mode 0, FIFO depth, device-table size
  - Synthesizable SystemVerilog, no gated clocks and no internal tri-states; DFT scan-mode reset control
  - Bare-metal C and Linux drivers

- Compliance:

  - MIPI I3C Basic v1.2 (with errata 01), and I3C Basic v1.1.1 behavior as a register option
  - MIPI I3C Conformance Test Suite (CTS) v1.2, public edition
  - NXP I2C-bus specification UM10204; AMBA APB

Verification Method

The core is delivered with a self-checking directed test suite: AMBA bus functional models, an independent I3C bus monitor that re-checks every SDR and HDR frame, and fault injection for the error paths. The dual-role core is tested back-to-back – one instance as Controller, one as Target, plus a third for Controller hand-off – and against third-party I3C Target models.

Release 1.2.0 grows the suite to about 165 tests, including the MIPI I3C CTS v1.2 tests, run in every build. Compliance is also checked with commercial MIPI I3C Verification IP.

Customer Evaluation

Digital Blocks offers a variety of methods for prospective customers to evaluate the DB-I3C-BASIC-MS-APB. Please contact Digital Blocks for additional information.

Deliverables

The DB-I3C-BASIC-MS-APB is available as synthesizable SystemVerilog RTL or an FPGA netlist, with Synopsys Design Constraints, the simulation test bench with expected results, a C++ model, bare-metal C and Linux drivers, and documentation: datasheet, Technical Reference Manual, Integration Guide, coverage report and CTS compliance report.

Ordering Information

Part numbers: DB-I3C-BASIC-MS-APB (Controller / Target), DB-I3C-BASIC-M-APB (Controller), DB-I3C-BASIC-S-APB (Target); AXI4-Lite versions on request.

Please contact Digital Blocks for additional technical, pricing, evaluation, and support information.

Digital Blocks, Inc.
PO Box 192
587 Rock Rd
Glen Rock, NJ 07452 USA
Phone: +1-551-258-0412
info@digitalblocks.com

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