General Description

The Digital Blocks DB-I3C-BASIC-S-APB IP Core interfaces a microprocessor via the AMBA APB Bus to an I3C Bus, compliant to the MIPI I3C Basic v1.2 Improved Inter Integrated Circuit specification. I3C Basic serves as an upgrade path to the I2C standard.

The I3C is a two-wire bidirectional interface standard (SCL is Clock, SDA is Data) for transfer of bytes of information between two or more compliant I3C devices as well as legacy I2C Slave devices.

The DB-I3C-BASIC-S-APB is a Target-only (Slave-only) implementation – the Controller role logic is removed for a smaller VLSI footprint – for applications requiring Target-Receiver and Target-Transmitter capability. An external I3C Controller supplies SCL and initiates all traffic; the core responds to SDR Private Write / Read and Direct CCC messages at its dynamically assigned address, and to the v1.2 High Data Rate modes HDR-DDR and HDR-BT including HDR-BT Multi-Lane. With a 12.5 MHz SCL the core reaches 12.5 Mbps in SDR, 25 Mbps in HDR-DDR and HDR-BT, and 50 / 100 Mbps in HDR-BT Multi-Lane x2 / x4.

In an ASIC / ASSP / FPGA integrated circuit the microprocessor is typically an ARM or RISC-V processor, but can be any embedded processor. Figure 1 depicts the system view of the DB-I3C-BASIC-S-APB IP Core embedded within an integrated circuit device with its microprocessor configuration.

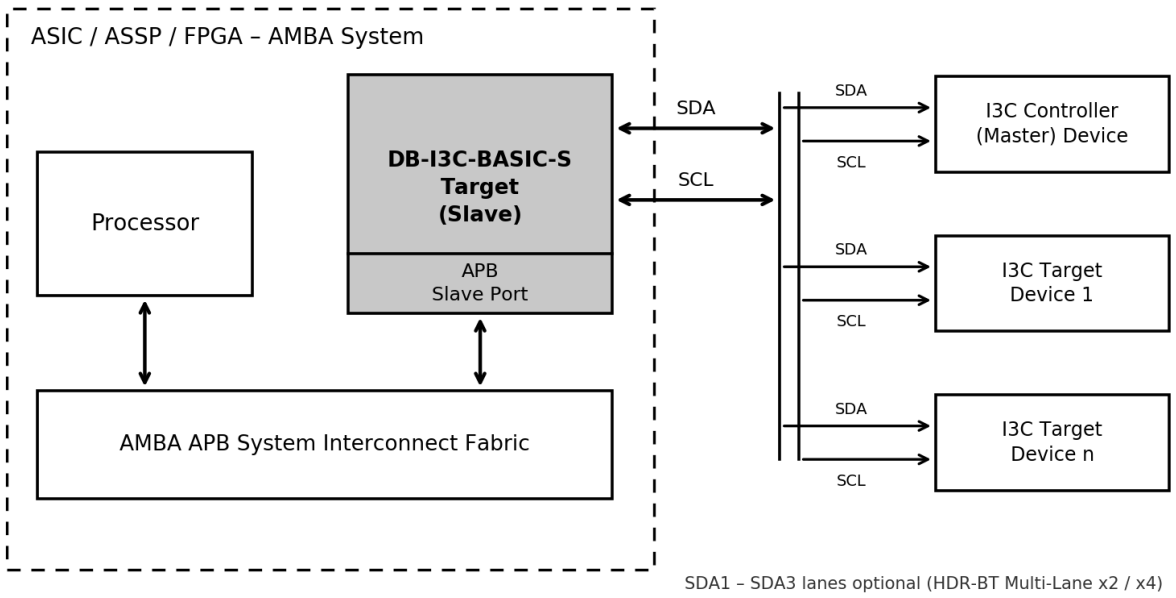

Figure 1: DB-I3C-BASIC-S-APB Target System Diagram

Features

- I3C Target (Slave) – implements the Target-only protocol for a smaller VLSI footprint, for applications requiring Target-Receiver and Target-Transmitter capability
- Supported I3C bus modes and data rates (clocked by the external Controller):
  - Single Data Rate (SDR) – up to 12.5 MHz SCL, 12.5 Mbps
  - HDR-DDR – 25 Mbps (2 bits per SCL period) at the same 12.5 MHz SCL
  - HDR-BT – 25 Mbps single lane
  - HDR-BT Multi-Lane – 50 Mbps (x2) / 100 Mbps (x4), build-time lane option
- I3C communications support:
  - I3C SDR Private Write / Read at the assigned dynamic address, with T-bit parity

  - Broadcast and Direct CCC reception and response
  - Received bytes are pushed to the RX FIFO and read data is served from the TX FIFO, with a per-message status word returned to software
- HDR (High Data Rate) modes, MIPI I3C Basic v1.2:
  - HDR-DDR (§6.2): hardware ENTHDR0 entry, HDR Restart Pattern between messages of one frame, and HDR Exit Pattern – 20-bit words with preamble, PA1/PA0 parity and CRC-5
  - HDR-BT / Bulk Transport (§6.4): 7-byte Header Block, 32-byte Data Blocks with ragged Last block, CRC Block with CRC-16 (mandatory) or CRC-32 (optional), receiver-driven termination in both directions, and zero-length writes
  - HDR-BT Multi-Lane (§6.7, Coding 0 Compatible Mode): data and CRC blocks striped over 2 or 4 lanes; all bus management stays on SCL / SDA0 for interoperability with single-lane devices
  - ENDXFER CCC flow-control options applied and read back through the SENDXFER register
  - MLANE CCC (0x2D / 0x9D) processing: Get-ML-Caps, lane-format Set / Get, and ML reset, with the active lane format readable in the SMLSR register
  - Error detection: preamble / framing, HDR-DDR parity and CRC-5, HDR-BT header parity, CRC-16 / CRC-32 and the Transition_Verify handshake – reported per message and in sticky HDR status registers with error counters
  - HDR modes are a build-time option (HDR_EN); with HDR removed the core is SDR-only and remains HDR-tolerant
- I3C compliant features:
  - I3C Characteristics Registers (BCR / DCR / PID), with GETCAPS reporting the built HDR-DDR, HDR-BT, CRC-32 and Multi-Lane capabilities and the BCR Advanced-Capabilities bit
  - Common Command Code (CCC) processor – broadcast ENEC, DISEC, RSTDAA, ENTDAA, ENTASx, SETMWL, SETMRL, ENDXFER, RSTACT, ENTHDRx, MLANE; direct SETNEWDA, SETMWL / GETMWL, SETMRL / GETMRL, GETBCR, GETDCR, GETPID, GETSTATUS, GETCAPS, ENDXFER, RSTACT, MLANE
  - Dynamic Address Assignment – ENTDAA participation with open-drain arbitration back-off and SETNEWDA re-assignment
  - In-Band Interrupt (IBI) request with payload, enabled / disabled by ENEC / DISEC
  - Hot-Join request, qualified by the bus-idle time
  - Target Reset Pattern detection with the RSTACT reset action
  - Max Write Length / Max Read Length / Max Data Speed and Status registers, updated by the corresponding CCCs
  - I3C error processing
- Dynamic addressing only – no legacy I2C static address response, so the core never claims the bus as an I2C Slave
- Parameterized FIFO memory for off-loading the I3C transfers from the processor:
  - Separate TX and RX FIFOs, parameterizable in depth (256 bytes by default) and width
  - Clock-domain crossing between the I3C SCL domain and the CPU clock is contained in the FIFOs and synchronizers
- System-level features & integration capabilities:
  - CPU interface to Control / Status Registers and the parameterized FIFO, with support for APB / AHB / AXI / AXI4-Lite / Avalon SoC interconnect fabrics (APB and AXI4-Lite delivered from the same RTL tree)
  - Internal interrupt controller (single interrupt to the embedded processor, with per-source mask and status registers)
  - Optional: DMA transfer between the I3C Bus and memory (SDRAM / SRAM / FLASH)
  - Build-time configuration: HDR_EN (HDR modes), Multi-Lane x1 / x2 / x4, FIFO depth, and CPU bus interface
- Fully-synchronous, synthesizable SystemVerilog RTL core with no gated clocks and no internal tri-states, for easy integration into FPGA or ASIC design flows. The SDR logic is rising-edge clocked; the HDR engines additionally use the falling SCL edge for dual-edge data (constraints supplied).
- Low power RTL design
- Compliance with I3C, I2C, and AMBA specifications:
  - MIPI Alliance – Specification for I3C Basic (Improved Inter Integrated Circuit), Version 1.2, public edition with errata 01
  - Verified against the MIPI Alliance I3C Conformance Test Suite (CTS) v1.2, public edition
  - AMBA APB

Pin Description

In addition to the AMBA APB Bus interface, which includes the input clock and reset and the output interrupt, the I3C bus interface signals are listed in Table 1. The I3C pads are driven with the Digital Blocks open-drain / push-pull

convention: an *_en output pulled low drives the line low, and the matching *_en_active_drv output selects push-pull drive for the I3C high phases. A bi-directional pad may be used for SDA / SCL by combining the enable and data outputs.

SCL is an input to the Target: the external I3C Controller supplies the clock, and the SCL drive outputs are kept released so the pin list matches the Controller and dual-role configurations for a common pad ring.

Name	Type	Description
AMBA APB Slave Interface		
db_i3c_slv_pclk	Input	APB clock (PCLK)
db_i3c_slv_presetn	Input	APB reset, active low (PRESETn)
db_i3c_slv_psel	Input	APB select
db_i3c_slv_penable	Input	APB enable
db_i3c_slv_pwrite	Input	APB write (1) / read (0)
db_i3c_slv_paddr[31:0]	Input	APB address
db_i3c_slv_pwdata[31:0]	Input	APB write data
db_i3c_slv_prdata[31:0]	Output	APB read data
intr	Output	Interrupt to the microprocessor
I3C Bus Interface (lane 0 – SDA / SCL)		
sdai	Input	Serial Data in, from the SDA pad
sdao	Output	Serial Data out (push-pull data)
sdao_en	Output	SDA open-drain drive-low enable, active low: 0 = pull SDA low
sdao_en_active_drv	Output	SDA push-pull enable, active high: 1 = actively drive sdao; 0 = open-drain / release
scli	Input	Serial Clock in, from the SCL pad
sclo_en	Output	SCL line state / drive-low enable, active low: 0 = pull SCL low, 1 = SCL high
sclo_en_active_drv	Output	SCL push-pull enable, active high: 1 = actively drive SCL high; 0 = release
I3C Multi-Lane Interface – optional, HDR-BT (lanes 1–3)		
sda1i, sda1o, sda1o_en, sda1o_en_active_drv	I / O	Lane 1 data and drive controls, same convention as lane 0. Present when DB_I3C_ML_DUAL or DB_I3C_ML_QUAD is defined (x2 / x4 builds).
sda2i, sda2o, sda2o_en, sda2o_en_active_drv, sda3i, sda3o, sda3o_en, sda3o_en_active_drv	I / O	Lanes 2 and 3 data and drive controls. Present when DB_I3C_ML_QUAD is defined (x4 builds). Lanes carry HDR-BT data and CRC blocks only and are push-pull; the default x1 build has the legacy pin list with no lane pins.

Table 1: DB-I3C-BASIC-S-APB – I/O Pin Description

Verification Method

The DB-I3C-BASIC-S-APB IP Core is delivered with a verification test suite containing AMBA bus functional models that program the control & status registers, generate and send I3C messages, monitor the I3C bus protocol and timing, and check expected results. The passive bus monitor independently re-decodes SDR, HDR-DDR and HDR-BT traffic (including the multi-lane striping) and re-computes parity, CRC-5, CRC-16 and CRC-32 as a second opinion on every frame; a fault-injection model corrupts selected bits to exercise the error paths.

The regression comprises 76 self-checking tests – directed SDR, 31 MIPI I3C CTS v1.2 tests, bridge, and HDR-DDR / HDR-BT – run on both the APB and the AXI4-Lite deliverables, plus 3 additional Multi-Lane tests in the x2 and x4 builds (79 tests). All tests pass in every configuration.

The Target is verified against the Digital Blocks I3C Controller IP and the MIPI CTS exerciser model on a wired-AND bus model with contention checking, covering dynamic addressing, CCCs, IBI, Hot-Join, Target Reset and all HDR modes.

Customer Evaluation

Digital Blocks offers a variety of methods for prospective customers to evaluate the DB-I3C-BASIC-S-APB. Please contact Digital Blocks for additional information.

Deliverables

The DB-I3C-BASIC-S-APB is available in synthesizable RTL SystemVerilog or a technology-specific netlist for FPGAs, along with Synopsys Design Constraints, a simulation test bench with expected results, datasheet, and user manual (Technical Reference Manual with the I3C Basic v1.2 HDR addendum). The same RTL tree delivers the APB and AXI4-Lite bus interfaces and the Controller-only, Target-only and dual-role configurations.

Ordering Information

Please contact Digital Blocks for additional technical, pricing, evaluation, and support information.

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