General Description

The Digital Blocks DB-I3C-FULL-MS-APB IP Core connects an embedded processor on the AMBA APB bus to an I3C bus, compliant with the MIPI I3C v1.1 specification. It builds on the Digital Blocks I3C Basic core and adds the features of the full I3C specification: the HDR Ternary modes HDR-TSP and HDR-TSL, Synchronous Timing Control, Device-to-Device Tunneling, Monitoring Device Early Termination, and Multi-Lane for SDR and HDR-DDR.

The core implements both I3C roles – Controller and Target – selected at run time, with Secondary Controller hand-off. At 12.5 MHz SCL it reaches 12.5 Mbps in SDR, 25 Mbps in HDR-DDR and HDR-BT, about 33 Mbps in HDR-TSP, and up to 100 Mbps with Multi-Lane x4.

Ternary receive needs a time reference, so the SoC supplies an always-on sampling clock of at least 100 MHz (200 MHz recommended) while HDR Ternary is enabled. Every full-specification feature is a build option, and a Basic-only build of the same RTL is an I3C Basic v1.2 device.

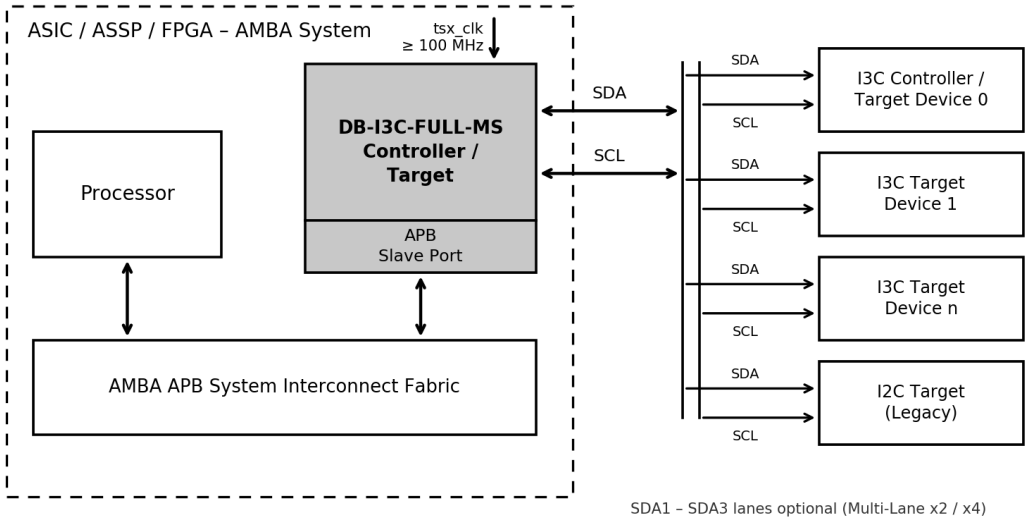


Figure 1: DB-I3C-FULL-MS-APB Controller / Target System Diagram

Features

- Dual-role MIPI I3C v1.1 Controller / Target, role selected at run time; Controller-only and Target-only configurations

- All DB-I3C-BASIC-MS-APB Rel 1.2.0 features: SDR, HDR-DDR, HDR-BT with Multi-Lane, Secondary Controller, device table, static and group addressing, error recovery, Asynchronous Timing Control Mode 0
- Bus modes and data rates at 12.5 MHz SCL:
  - SDR – 12.5 Mbps; legacy I2C devices on the same bus
  - HDR-DDR – 25 Mbps
  - HDR-TSP / HDR-TSL (ternary) – about 33 Mbps
  - HDR-BT – 25 Mbps; Multi-Lane x2 / x4 – 50 / 100 Mbps
  - SDR and HDR-DDR Multi-Lane x2 / x4 – build option
- HDR Ternary (HDR-TSP, and HDR-TSL for buses with legacy I2C devices):
  - Controller and Target, including CCCs and flow control in ternary mode
  - Target receive sampled by an always-on clock: 100 MHz minimum, 200 MHz or 100 MHz both-edge sampling recommended; decode window programmable
  - Clock tree gated inside the core until a ternary transfer starts (planned)
- Timing Control:
  - Synchronous mode – Controller SYNC ticks and Target event time stamps
  - Asynchronous Mode 0 – time-stamped In-Band Interrupts
- Device-to-Device Tunneling: Target-to-Target data through the Controller's tunneling CCC, with the core as source or receiver
- Monitoring Device Early Termination: a monitoring device can stop a transfer in progress; Controller support for the resulting arbitration
- Specification profile: I3C v1.1 by default, I3C Basic v1.2 behavior selectable by register on the same netlist
- Separate TX and RX FIFOs, parameterized (256 bytes by default)
- Integration:
  - APB, or AXI4-Lite from the same RTL
  - Single interrupt with per-source mask and status
  - Build options for each full-specification feature; Basic-only build
  - Synthesizable SystemVerilog; constraints supplied for the SCL, time-stamp and ternary sampling clock domains; DFT scan-mode reset control
  - Bare-metal C and Linux drivers, including HDR-DDR and HDR Ternary transfers in the Linux I3C subsystem
- Compliance:
  - MIPI I3C Specification v1.1 (full), with v1.1.1 errata
  - MIPI I3C Basic v1.2 in the Basic-only build; MIPI I3C CTS

- NXP I2C-bus specification UM10204; AMBA APB

Verification Method

The core extends the DB-I3C-BASIC-MS-APB test suite. Ternary transfers are checked against an independent wire-level model with SCL / SDA skew and edge-rate sweeps at each supported sampling clock; tunneling and early termination are checked with three devices on the bus.

Compliance is checked with commercial Verification IP for MIPI I3C v1.1, and every v1.1 requirement in the full-only features is traced to a test. FPGA validation uses an I3C protocol analyzer with HDR Ternary decode.

Customer Evaluation

Digital Blocks offers a variety of methods for prospective customers to evaluate the DB-I3C-FULL-MS-APB. Please contact Digital Blocks for additional information.

Deliverables

The DB-I3C-FULL-MS-APB is available as synthesizable SystemVerilog RTL or an FPGA netlist, with Synopsys Design Constraints, the simulation test bench with expected results, a C++ model, bare-metal C and Linux drivers, and documentation: datasheet, Technical Reference Manual, Integration Guide, coverage report and compliance report.

Ordering Information

Part numbers: DB-I3C-FULL-MS-APB (Controller / Target), DB-I3C-FULL-M-APB (Controller), DB-I3C-FULL-S-APB (Target); AXI4-Lite versions on request.

Please contact Digital Blocks for additional technical, pricing, evaluation, and support information.

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