General Description

The Digital Blocks DB-I3C-HCI-APB IP Core is an I3C Controller with the MIPI I3C Host Controller Interface (HCI) v1.2 register model. Because the register model is standard, the core runs under standard HCI software, such as the Linux mipi-i3c-hci driver, with no custom driver.

Command descriptors written by software are turned into I3C transfers by the Digital Blocks I3C Controller engine, compliant with MIPI I3C Basic v1.2: SDR up to 12.5 Mbps, HDR-DDR at 25 Mbps, and legacy I2C. Address assignment, In-Band Interrupts, Hot-Join, Target Reset and bus recovery run in hardware.

Release 1 moves data by programmed I/O (PIO) through an APB or AXI4-Lite register port. Release 2 adds DMA through an AXI4 manager, as shown in Figure 1.

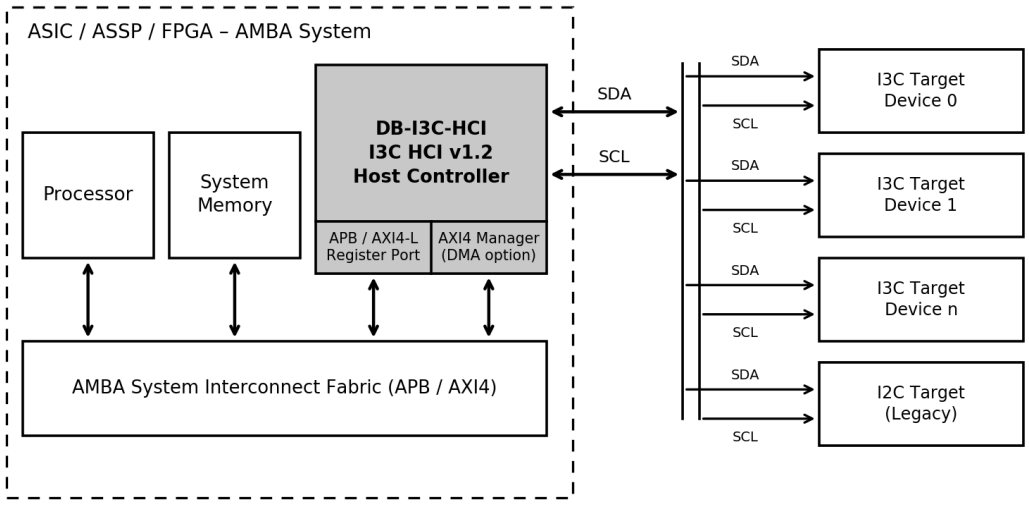


Figure 1: DB-I3C-HCI-APB Host Controller System Diagram

Features

- MIPI I3C HCI v1.2 Host Controller:
  - Standard capability, operation and interrupt registers; Device Address Table and Device Characteristics Table
  - PIO data transfer: command, response, TX / RX data and IBI queues
  - DMA option (Release 2): command / response rings, scatter-gather data buffers and IBI rings through a 64-bit AXI4 manager

- I3C bus: SDR at all speed modes, HDR-DDR, and legacy I2C devices
- Bus management in hardware:
    - Dynamic address assignment (ENTDAA) and SETDASA from the Device Address Table
    - In-Band Interrupts with payload; Hot-Join; automatic reject and disable of unwanted requests
    - CCCs with defining bytes, and automatic retry after a NACK
    - Target Reset, and bus recovery: stuck-SDA recovery, forced STOP, HDR Exit
    - Auto-Command: reads issued automatically on Pending Read notifications
- Error handling: halt on error and resume, abort, and command-sequence timeout detection
- Planned options: IBI time stamping and credit counting; combined and scheduled commands; Standby Controller Mode and Dead Bus Recovery
- Digital Blocks extended capability for HDR-BT and Multi-Lane x2 / x4, outside the standard HCI driver
- Parameterized queues and tables: command / response 16 entries, TX / RX data and IBI 64 DWORDs, Device Address Table 32 and Device Characteristics Table 8 entries by default
- Integration:
    - APB with byte strobes, or AXI4-Lite, register port; AXI4 manager for DMA
    - Single interrupt
    - Synthesizable SystemVerilog; DFT scan-mode reset control
- Software:
    - Linux: the upstream mipi-i3c-hci driver in the Linux I3C subsystem, with a device-tree fragment
    - Bare-metal C driver
- Compliance:
    - MIPI I3C HCI v1.2 and MIPI I3C TCRI v1.0
    - MIPI I3C Basic v1.2 bus behavior; NXP I2C-bus specification UM10204
    - AMBA APB, AXI4-Lite and AXI4

Verification Method

The test suite drives the core through a model of the HCI software flows – PIO queues and, for DMA, rings in a host-memory model – and checks every bus frame, response and IBI against expected results. The I3C bus side uses the Digital Blocks I3C Target, third-party Target models, and commercial MIPI I3C Verification IP as Targets and protocol checker.

Hardware validation runs the upstream Linux mipi-i3c-hci driver on an FPGA platform with real I3C devices and a protocol analyzer.

Customer Evaluation

Digital Blocks offers a variety of methods for prospective customers to evaluate the DB-I3C-HCI-APB. Please contact Digital Blocks for additional information.

Deliverables

The DB-I3C-HCI-APB is available as synthesizable SystemVerilog RTL or an FPGA netlist, with Synopsys Design Constraints, the simulation test bench with expected results, a bare-metal C driver, a Linux device-tree fragment and integration note, and documentation: datasheet, Technical Reference Manual, Integration Guide and coverage report.

Ordering Information

Part numbers: DB-I3C-HCI-APB and DB-I3C-HCI-AXI4L (PIO), DB-I3C-HCI-AXI4-DMA (PIO and DMA).

Please contact Digital Blocks for additional technical, pricing, evaluation, and support information.

Digital Blocks, Inc.
PO Box 192
587 Rock Rd
Glen Rock, NJ 07452 USA
Phone: +1-551-258-0412
info@digitalblocks.com

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