

General Description

The Digital Blocks DB-I3C-M-APB Controller IP Core interfaces a microprocessor via the AMBA APB Bus to an I3C Bus, compliant to the MIPI I3C ó Improved Inter Integrated Circuit specification.

The I3C is a two-wire bidirectional interface standard (SCL is Clock, SDA is Data) for transfer of bytes of information between two or more compliant I3C devices as well as legacy I2C Slave devices.

The DB-I3C-M-APB is an I3C Master Controller supporting I3C SDR / Broadcast / Direct Messages, Legacy I²C Message, and I3C HDR Mode (optionally).

In an ASIC / ASSP / FPGA integrated circuit, typically, the microprocessor is an ARM, MIPS, or RISC-V processor, but can be any embedded processor. Figure 1 depicts the system view of the DB-I3C-M-APB Controller IP Core embedded within an integrated circuit device with its Microprocessor Configuration.

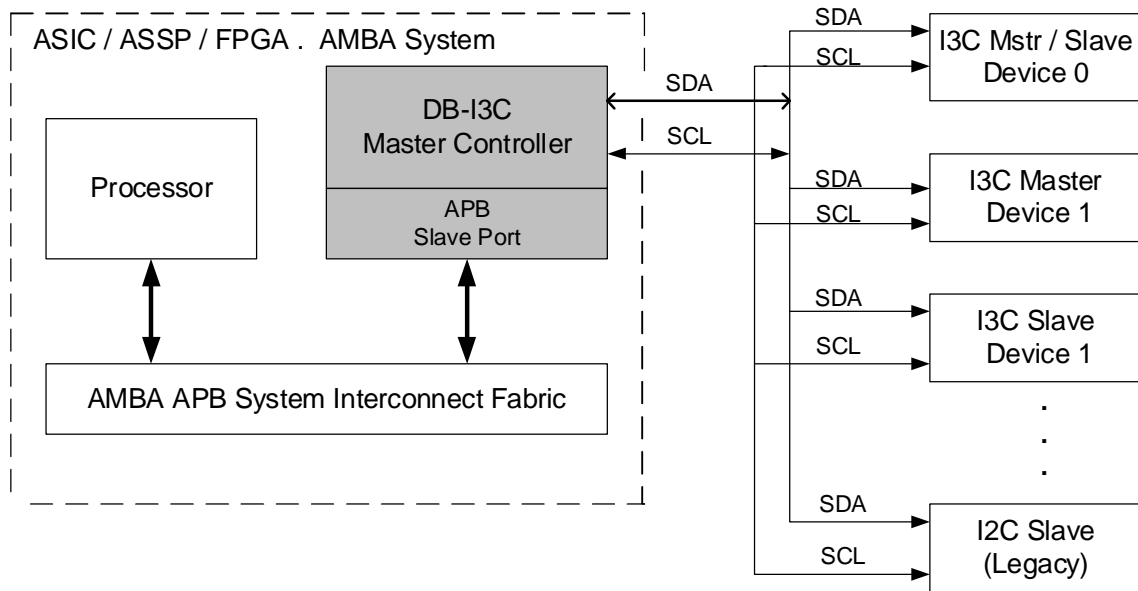


Figure 1: DB-I3C-M-APB Controller ó System Diagram

Features

- Master MIPI I3C Controller
- Supports following I3C bus speeds:
 - Single Data Rate (SDR) - up to 12.5 MHz
 - High Data Rate (HDR) (Optional)
- I3C Communications Support:
 - I3C SDR / Broadcast / Direct Messages
 - Legacy I²C Message
 - I3C HDR Mode (optional)
- I3C compliant features:
 - Dynamic Addressing Assignment
 - Secondary Master Function
 - In-Band Interrupt
 - Hot-Join Mechanism
 - Synchronous/ Asynchronous Timing Stamping
 - I3C Characteristics Registers
 - Common Command Codes (CCCs)
- Parameterized FIFO memory for off-loading the I3C transfers from the processor:
 - Targets embedded processors with the I3C Controller independently controlling the I3C Message Transmit/Receive with bytes of information buffered to and from a FIFO.
 - Dual Clock FIFO, decoupling APB bus & I3C clock domains
 - FIFO parameterizable in depth and width
- System-level features & integration capabilities:
 - CPU Interface to Control / Status Registers & parameterized FIFO with support for APB / AHB / AXI / AXI-lite / Avalon SoC Interconnect fabrics
 - Internal Interrupt Controller (Interface to embedded processor)
- Optional system-level features & integration capabilities:
 - DMA transfer between the I3C Bus & Memory (SDRAM / SRAM / FLASH)
- Compliance with I3C, I²C, and AMBA specifications:
 - MIPI Alliance ó Specification for I3C ó Improved Inter Integrated Circuit, Version 1.0, 23 December 2016 (doc õmipi_I3C_specification_v1-0ö)
 - Philips/NXP ó The I2C-Bus Specification, Version 2.1, January 2000 and UM10204 Rev 6 ó 4 April 2014
 - Compliance with AMBA Specification ó APB

- Fully-synchronous, synthesizable Verilog RTL core, with rising-edge clocking, no gated clocks, and no internal tri-states, for easy integration into FPGA or ASIC design flows.
- Low Power Verilog RTL design

Pin Description

In addition to the AMBA APB Bus interfaces, which include the input CLOCK and RESET and output INTR (interrupt) signals, the I3C interface signals list in Table 1.

Name	Type	Description
I3C Bus interface		
SDAI	Input	Serial Data
SDAO	Output	Serial Data
SCLI	Input	Serial Clock Line
SCLO	Output	Serial Clock Line

Table 1: DB-I3C-M-APB – I/O Pin Description

Verification Method

The DB-I3C-M-APB Controller IP Core contains a verification test suite with AMBA APB Bus functional models that program the DB-I3C-M-APB control & status registers, generates & sends I3C messages, monitors the I3C bus protocol and timing, and checks expected results.

Customer Evaluation

Digital Blocks offers a variety of methods for prospective customers to evaluate the DB-I3C-M-APB. Please contact Digital Blocks for additional information.

Deliverables

The DB-I3C-M-APB is available in synthesizable RTL Verilog and a technology-specific netlist for FPGAs, along with Synopsys Design Constraints, a simulation test bench with expected results, datasheet, and user manual.

Ordering Information

Please contact Digital Blocks for additional technical, pricing, evaluation, and support information.

Digital Blocks, Inc.

DB-I3C-M-APB
AMBA APB Bus MIPI I3C Controller

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