General Description

The DB-I3C-S-SCL-CLK-REG is an I3C Slave Controller IP Core focused on low power, low noise, low VLSI footprint ASIC / ASSP designs requiring the configuration & control of registers with no free running clock. The DB-I3C-S-SCL-CLK-REG processes the I3C protocol & physical layers, and receives & transmits bytes with respect to the I3C payload to / from User Registers within an ASIC / ASSP / FPGA device. The DB-I3C-S-SCL-CLK-REG Controller implements the Slave-Transmit and Slave-Receive protocol according to the MIPI I3C-Basic-Spec-ver1_0 specification.

The DB-I3C-S-SCL-CLK-REG builds on Digital Blocks DB-I2C-S-SCL-CLK Controller and supports I2C Master Slave-Transmit and Slave-Receive protocol according to the Philips I2C-Bus Specification, Version 2.1 as well as the updated NXP Rev .5 October 9, 2012 Specification.

Figure 1 depicts the system view of the DB-I3C-S-SCL-CLK-REG Controller IP Core embedded within an ASIC, ASSP or FPGA device. The DB-I3C-S-SCL-CLK-REG Controller receives and transmits data with respect to an external I3C or I2C Master Controller. The DB-I3C-S-SCL-CLK-REG internally interfaces to User Registers / Memory.

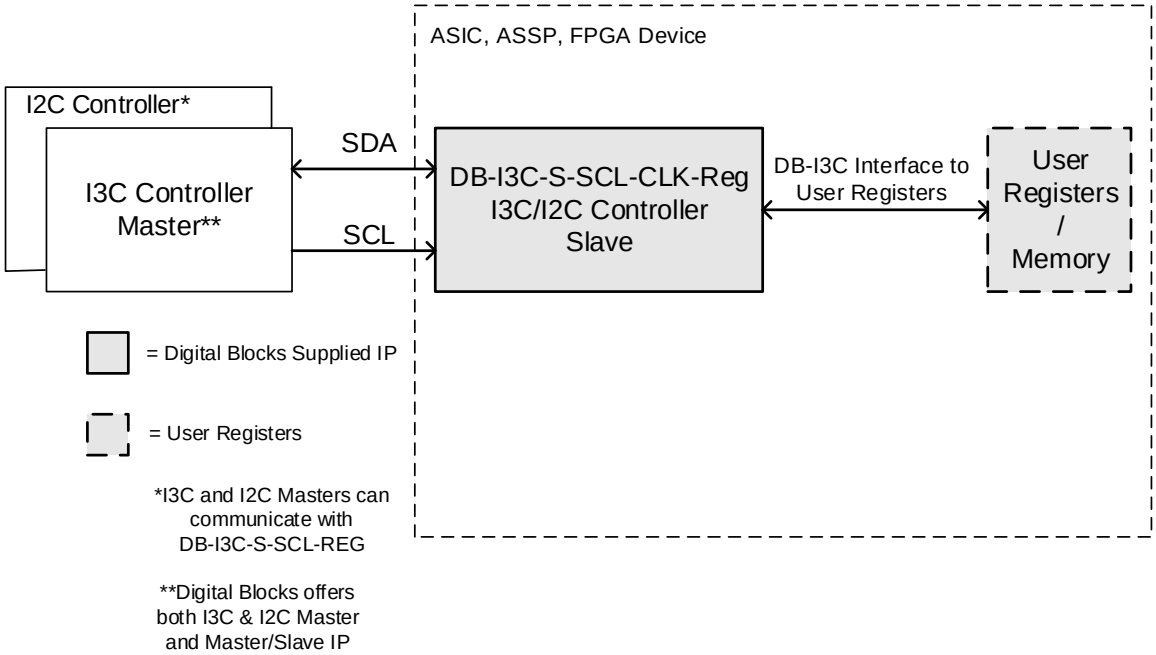

Figure 1: DB-I3C-S-SCL-CLK-REG Controller - System View

I3C Features

- I3C Slave Controller - Implements Slave-only protocol for smaller VLSI footprint, for applications requiring Slave–Receiver and Slave–Transmitter capability
- SCL Clock only for low power, low noise applications requiring configuration & management of User Registers / Memory
- Autonomous I3C Slave Controller:
    - No local CPU host required
    - No configuring of control/status registers
- Supports I3C SDR up to 12.5 MHz bus speed
- I3C 7-bit Dynamic Address Assignment
- I3C CCC Command Processor
- Compliance with I3C specification for I3C SDR Slave
    - MIPI Alliance – I3C-Basic-Spec-ver1_0 specification

I2C Features

- I2C Slave Controller - Implements Slave-only protocol for smaller VLSI footprint, for applications requiring Slave–Receiver and Slave–Transmitter capability
- I^2C 7- or 10-bit addressing
- Supports five I^2C bus speeds:
    - Standard mode (100 Kb/s)
    - Fast mode (400 Kb/s)
    - Fast mode plus (1 Mbit/s)
    - Ultra fast mode (5 Mbit/s)
    - Hs-mode (3.4 Mbit/s)
- Compliance with I2C specifications:
    - Philips – The I2C-Bus Specification, Version 2.1, January 2000
    - NXP Rev .5 October 9, 2012
- Fully-synchronous, synthesizable Verilog RTL core. Easy integration into FPGA or ASIC design flows.

Pin Description

The DB-I3C-S-SCL-CLK-REG I3C Slave Controller interface signals are listed in Table 1. Note that a bi-directional driver is available for SDAI / SDAO.

Name	Type	Description
I3C Bus Interface		
SDAI	Input	Serial Data
SDAO	Output	Serial Data
SCLI	Input	Serial Clock Line
User Register Interface		
Please contact Digital Blocks for more information		

Table 1: DB-I3C-S-SCL-CLK-REG – I/O Pin Description

Verification Method

The DB-I3C-S-SCL-CLK-REG Controller IP Core contains a test suite that generates & sends I3C transactions, monitors the I3C bus protocol, and checks expected results.

The DB-I3C-S-SCL-CLK-REG Controller IP Core has internally been verified as follows:

- Instantiated within an FPGA, and communicating with ASSP I3C Master IP Controllers.
- Instantiated within an FPGA, and communicating with Digital Blocks I3C Master IP Controller, and A NIOS II processor for expected data checking.
- Customer Implementations

Customer Evaluation

Digital Blocks offers a variety of methods for prospective customers to evaluate the DB-I3C-S-SCL-CLK-REG. Please contact Digital Blocks for additional information.

Deliverables

The DB-I3C-S-SCL-CLK-REG is available in synthesizable RTL Verilog or a technology-specific netlist for FPGAs, along with Synopsys Design Constraints, a simulation test bench with expected results, datasheet, and user manual.

Ordering Information

Please contact Digital Blocks for additional technical, pricing, evaluation, and support information.

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