General Description

The DB-I3C-Target-Bridge-to-AMBA is an Autonomous I3C Slave (Target) to APB or AXI4-Lite Master Bridge IP Core. It allows an external I3C Controller (Master) to read and write a User System's APB/AXI4-Lite address space directly over the I3C bus - with no local CPU host and no configuration or control/status registers. Device identity (48-bit Provisional ID, BCR, DCR, optional I2C static address) is set by input straps or synthesis parameters; the bridge is operational at power-up.

The bridge implements the MIPI I3C Basic v1.2 SDR Slave protocol, building on the Digital Blocks DB-I3C-BASIC-MS Controller family Target engine. An I3C Private Write transfers a register/memory address followed by write data; an I3C Private Read (address phase then Repeated START read) returns data fetched over the APB/AXI4-Lite Master port. Multi-byte transfers auto-increment the address, enabling efficient block access. The architecture follows the proven Digital Blocks DB-I2C-S-REG-AXI autonomous I2C bridge, extended to I3C Basic v1.2 with Dynamic Address Assignment, CCCs, In-Band Interrupts, Hot-Join, and Target Reset.

Figure 1 depicts the system view of the DB-I3C-Target-Bridge-to-AMBA Bridge IP Core embedded within an ASIC, ASSP or FPGA, connecting an external I3C Controller to the User System via the on-chip APB/AXI4-Lite interconnect.

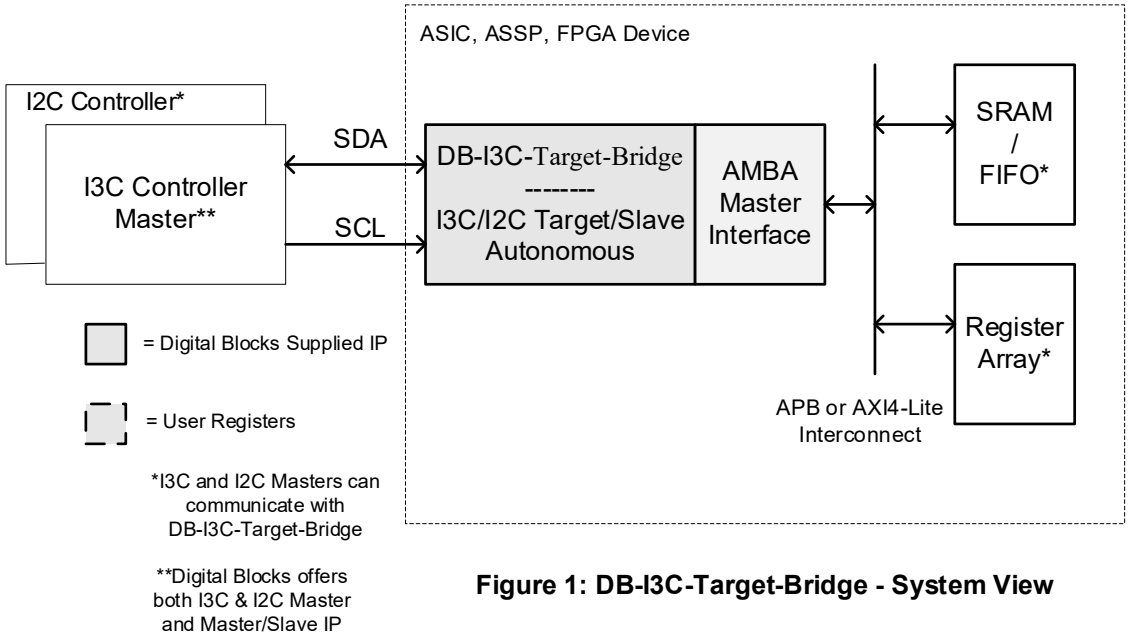

Figure 1: DB-I3C-Target-Bridge - System View

I3C Features

- I3C Target (Slave) Controller - implements Slave-only protocol for a smaller VLSI footprint, for applications requiring Slave-Receiver and Slave-Transmitter capability:
  - Slave-Receiver: I3C Private Write transfers accepted at the assigned Dynamic Address, with T-bit odd-parity checking on every byte
  - Slave-Transmitter: I3C Private Read transfers served at the assigned Dynamic Address, with T-bit continuation / end-of-data signaling
  - No Controller (Master) logic instantiated - minimal gate count and verification surface
- SCL-clock-only protocol engine for low power, low noise applications requiring configuration & management of User Registers / Memory:
  - Source-synchronous design: the I3C protocol engine is clocked directly by the SCL pin - no free-running oversampling clock, no PLL
  - Bus-side logic toggles only during I3C bus transactions; between frames the engine is quiescent for minimal dynamic power and EMI
  - Bus-clock domain (APB PCLK / AXI ACLK) crossing via gray-code-pointer dual-clock FIFOs - no timing dependency between the I3C bus rate and the system clock rate
- Autonomous I3C Slave Controller:
  - No local CPU host required
  - No configuring of control/status registers - operational at power-up
  - Device identity set by input straps / synthesis parameters: 48-bit Provisional ID (CFG_PID), Bus Characteristics Register (CFG_BCR), Device Characteristics Register (CFG_DCR), optional I2C static address (CFG_SADDR)
  - Register-address width (1 to 4 address bytes) and read-prefetch depth set by synthesis parameters
- Supports I3C SDR up to 12.5 MHz bus speed:
  - Push-pull SDR data phases at the full bus rate
  - Open-drain arbitration phases (address header ACK, ENTDAA, IBI, Hot-Join) per the I3C Basic specification
- I3C 7-bit Dynamic Address Assignment:

  - ENTDAA participation with 64-bit open-drain arbitration of PID / BCR / DCR against other Targets on the bus
  - DA parity check on the assigned address; retry on subsequent ENTDAA rounds after arbitration loss
  - SETNEWDA (Controller reassigns the Dynamic Address) and RSTDAA (return to unassigned) supported

- I3C CCC Command Processor (broadcast and direct):
  - ENEC / DISEC - event enable/disable (IBI, Hot-Join)
  - ENTAS0-ENTAS3 - activity state selection
  - SETMWL / SETMRL, GETMWL / GETMRL - Max Write/Read Length, retained as internal CCC-writable state (no CPU involvement)
  - GETPID, GETBCR, GETDCR - identity retrieval from the strap values
  - GETSTATUS - v1.2 format status, including bridge Protocol Error reporting (bus-master error responses)
  - GETCAPS - v1.2 capabilities format
- In-Band Interrupt (IBI):
  - Initiated by the User System interrupt input (USER_IRQ pin)
  - IBI with Mandatory Data Byte (MDB) per the v1.2 BCR[2] rules
  - Open-drain arbitrated header; honors ENEC/DISEC state and Controller ACK/NACK
- Hot-Join:
  - tIDLE-compliant (200 us) Hot-Join request generation for late bus attach; leads the Controller to run ENTDAA
- Target Reset Pattern (I3C Basic v1.2):
  - Detects the SDA-toggling-while-SCL-low reset pattern and asserts a reset output to the User System
  - HDR Exit Pattern tolerated (detected and ignored) per specification
- Compliance with I3C specification for I3C SDR Slave:
  - MIPI Alliance - I3C Basic Specification v1.2 (Public Release, ER01)
  - Interoperable with I3C Basic v1.0 / v1.1 Controllers for the SDR Slave feature set

Bridge Transaction Features

- Register/Memory Write: I3C Private Write payload = [register address byte(s)] + [data byte(s)] converted directly to bus-master write(s)
- Register/Memory Read: I3C Private Write of the register address, then Repeated START + Private Read streams read data back to the I3C Controller with T-bit continuation
- Programmable register-address width: 1 to 4 address bytes (8/16/24/32-bit address space), LSB-first on the wire
- Address auto-increment (+4, 32-bit word stride) for efficient multi-byte block transfers in both directions
- Byte-to-word packing and unpacking with byte-lane strobes for unaligned leading/trailing bytes
- Read prefetch: the bridge fetches ahead on completion of the address phase, hiding interconnect latency inside the Sr + header window; prefetch depth is a synthesis parameter
- Not-ready read policy: header NACK (spec-legal) - the Controller retries; no clock stretching exists in I3C and none is required
- Address-persistence strap: register address counter retained across STOP for split (STOP-separated) write-address / read transactions

AMBA Bus Master Features

- DB-I3C-Target-Bridge-to-APB - AMBA APB Master port:
  - APB3 protocol: SETUP -> ACCESS with PREADY wait-state support
  - PSLVERR capture: bus error terminates the transfer and is reported in GETSTATUS (Protocol Error) and on the error interrupt output
  - PSTRB byte lanes for partial-word writes
- DB-I3C-Target-Bridge-to-AXI4-Lite - AMBA AXI4-Lite Master port:
  - Independent read (AR/R) and write (AW/W/B) channels, single outstanding transaction
  - SLVERR / DECERR responses terminate the transfer and are reported in GETSTATUS (Protocol Error) and on the error interrupt output
  - WSTRB byte lanes for partial-word writes

- Identical I3C feature set and bridge transaction model across both bus variants - only the bus-master module differs

I2C Features

- Legacy I2C Slave operation at a strapped static address (CFG_SADDR) for pre-Dynamic-Address or mixed I2C/I3C bus systems
- Supports I2C bus speeds: Standard mode (100 Kb/s), Fast mode (400 Kb/s), Fast mode plus (1 Mb/s)
- 50 ns spike filter behavior per I2C on mixed buses; filter bypassed in I3C modes per the I3C Basic specification
- Compliance: NXP UM10204 I2C-bus specification Rev. 7 / Philips I2C-Bus Specification v2.1

User System Interface Features

- USER_IRQ input: one pin arms an IBI with Mandatory Data Byte - the User System raises interrupts to the remote I3C Controller with no local software
- TGT_RESET output: Target Reset Pattern detection drives a reset output to the User System
- BRG_ERROR interrupt output: bus-master error responses (PSLVERR / SLVERR / DECERR) flagged to the User System
- Identity straps sampled at reset - tie-off constants or board/package-level configuration

Implementation Features

- Fully-synchronous, synthesizable Verilog/SystemVerilog RTL core; easy integration into FPGA or ASIC design flows
- Two clock domains only (system bus clock + SCL pin); SDC timing constraints provided (clock groups, gray-code FIFO and quasi-static-configuration exceptions)
- No PLL, no oversampling clock, no analog cells required; standard open-drain / push-pull pad control outputs (uni-directional signals for bi-directional pad assembly)
- Verification: directed-test regression with per-test coverage (QuestaSim UCDB merge), Verilator lint sign-off, and third-party interoperability testing against an independent I3C Target/Controller implementation

Pin Description

The DB-I3C-Target-Bridge-AMBA I3C Slave Controller interface signals are listed in Table 1.

Name	Type	Description
I3C Bus Interface		
SDAI	Input	Serial Data input from pad
SDAO	Output	Serial Data push-pull data value
SDAO_EN	Output	Serial Data open-drain drive-low enable (active low)
SDAO_EN_ACTIVE_DRV	Output	Serial Data push-pull driver enable (active high)
SCLI	Input	Serial Clock input from pad (Target never drives SCL)
Identity/Configuration Straps		
CFG_PID[47:0], CFG_BCR, CFG_DCR, CFG_SADDR ({SA, enable}), CFG_ADR_PERSIST		
User System Sideband		
USER_IRQ + USER_IRQ_MDB[7:0] (IBI trigger + Mandatory Data Byte), TGT_RESET, BRG_ERROR		
AMBA Clocks/Reset		
APB or AXI-Lite CLK, RESETN		
APB Master Port (to-APB variant)		
M_PADDR/PSEL/PENABLE/PWRITE/PWDATA/PSTRB/PRDATA/PREADY/PSLVERR		
AXI4-Lite Master Port (to-AXI4-Lite variant)		
full AW/W/B + AR/R channels with WSTRB and RRESP/BRESP		

Table 1: DB-I3C-Target BRIDGE-AMBA - I/O Pin Description

Verification Method

The DB-I3C-Target-Bridge-AMBA Bridge IP Core is verified with the Digital Blocks I3C directed regression environment: a two-device open-drain bus model with protocol monitor, driven by the Digital Blocks DB-I3C-BASIC-MS Controller and cross-checked against an independent third-party I3C Target implementation (VIP). Directed tests cover private read/write bridging with auto-increment, ENTDAA, CCCs, IBI, Hot-Join, Target Reset, legacy I2C, and APB error responses, with per-test UCDB code coverage merged for sign-off

Customer Evaluation

Digital Blocks offers a variety of methods for prospective customers to evaluate the DB-DB-I3C-Target-Bridge-AMBA. Please contact Digital Blocks for additional information.

Deliverables

The DB-I3C-Target-Bridge-AMBA is available in synthesizable RTL SystemVerilog or a technology-specific netlist for FPGAs, along with Synopsys Design Constraints, a simulation test bench with expected results, TRM specification, and ASIC/FPGA integration guide.

Ordering Information

Please contact Digital Blocks for additional technical, pricing, evaluation, and support information.

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