General Description

The Digital Blocks DB-RTP-UDP-IP Intellectual Property Core is an RTP/UDP/IP Protocol Hardware Stack with the following protocol processing units:

- RTP Packet Processor
- UDP Packet Processor
- IP Packet Processor
- MAC Frame Layer Processor

Figure 1 depicts the RTP/UDP/IP Protocol Hardware Stack SoC IP Core embedded within an FPGA/ASSP/ASIC device. There are separate releases for 10/100/100 Mbps and 10/25 Gbps Ethernet MAC.

For RX (i.e., receiving packets from the network), there is optional packet reordering to absorb network jitter. For both TX/RX, multiple video streams supported.

The DB-RTP-UDP-IP-AV targets raw, uncompressed RGB/YUV video streams. See DB-RTP-UDP-IP-NAL for H.264 NAL Streams.

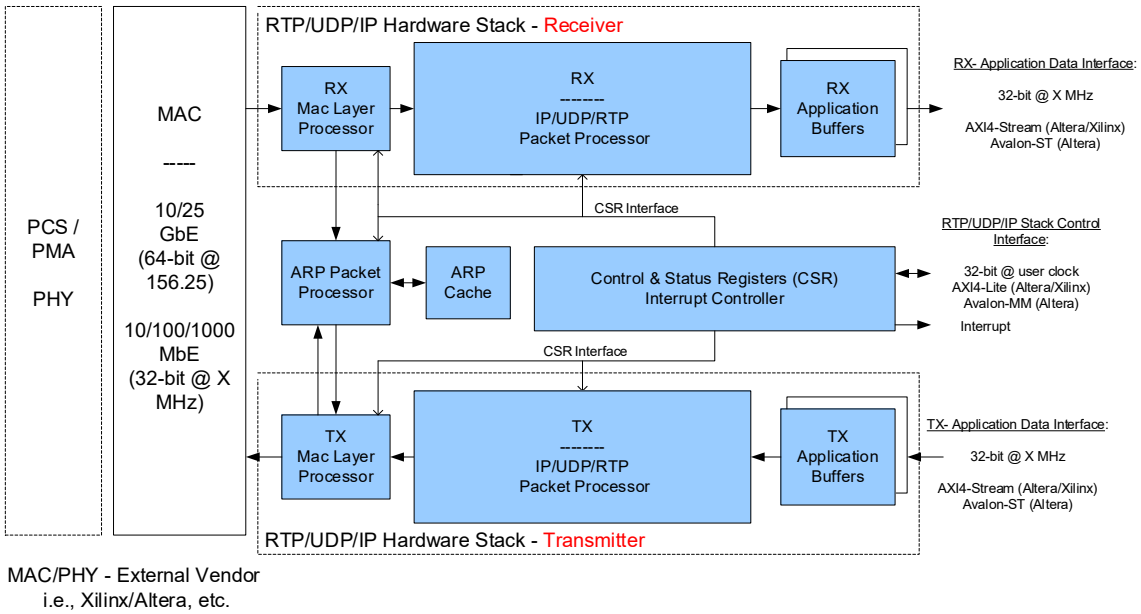

Figure 1: DB-RTP-UDP-IP-AV – RTP/UDP/IP Hardware Stack for Video Applications

Features

- RTP/UDP/IP Protocol Hardware Stack with separate releases:
  - 10/100/1000 MbE
  - 10/25 GbE
- Targets raw, uncompressed RGB/YUV video streams. See DB-RTP-UDP-IP-NAL for H.264 NAL Streams
- Internet Protocol (IP) Packet Processor:
  - IPv4 and IPv6 (optional) & ICMP (Internet Control Message Protocol) Protocol
  - IP header checksum generator (transmitter) & check (receiver), user-selectable Maximum Transmission Unit (MTU), Unicast, Broadcast & Multicast Packet support
  - Compliance with IETF IPv4/IPv6 RFCs
- User Datagram Protocol (UDP) Packet Processor:
  - UDP header checksum generator (transmitter) & check (receiver) – programmable on/off
  - Compliance with IETF UDP RFCs
- Real Time Transport Protocol (RTP) Packet Processor
  - Multiple TX/RX video streams supported
  - For RX, optional Packet reordering to absorb network jitter
  - Compliance with IETF RTP RFCs
- Address Resolution Protocol (ARP) Packet Processor (client/server) with 4-16 entry ARP cache
- High Speed Data Interface to user Host Application (typical clock rates):
  - 10/25 GbE: 64-bit @ 156.25 MHz, AXI4-Stream or Avalon-ST
  - 10/100/1000 MbE: 32-bit @ 2.5/25/125 MHz, AXI4-Stream or Avalon-ST
- Host set-up & control via Control & Status Registers and Interrupt Controller
  - 32-bit @ user clock rate AXI4-Lite or Avalon-MM
  - Optional hardwired no-register setup
- Pipeline, High Clock Rate, Low Latency architecture & design
- Fully synchronous, synthesizable RTL Verilog SoC IP core

Customer Evaluation

Digital Blocks offers a variety of methods for prospective customers to evaluate the RTP/UDP/IP Protocol Hardware Stack SoC IP Core. Please contact Digital Blocks for additional information.

Deliverables

The DB-RTP-UDP-IP-AV IP Core is available in synthesizable RTL Verilog or a technology-specific netlist for FPGAs, along with Synopsys Design Constraints, a simulation test bench with expected results, datasheet, and user manual.

Ordering Information

Please contact Digital Blocks for additional technical, pricing, evaluation, and support information.

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