

General Description

The Digital Blocks DB-RTP-UDP-IP-AV IP Core is a RTP/UDP/IP Protocol Hardware Stack with MAC Layer Pre- & Post-Processing and an ARP Packet Processor targeting low latency, full off-load from a processor, of Audio/Video Packet Processing. The DB-RTP-UDP-IP-AV is a Verilog SoC IP Core targeting Xilinx/Altera/Lattice FPGAs and ASIC/ASSP devices.

Figure 1 depicts the RTP/UDP/IP Protocol Hardware Stack SoC IP Core embedded within an FPGA/ASSP/ASIC device, connected on one side to a 10/100 MbE or 1/10/40 Gigabit Ethernet MAC, and on the other side to the user application, such as H.264/H.265 CODECs.

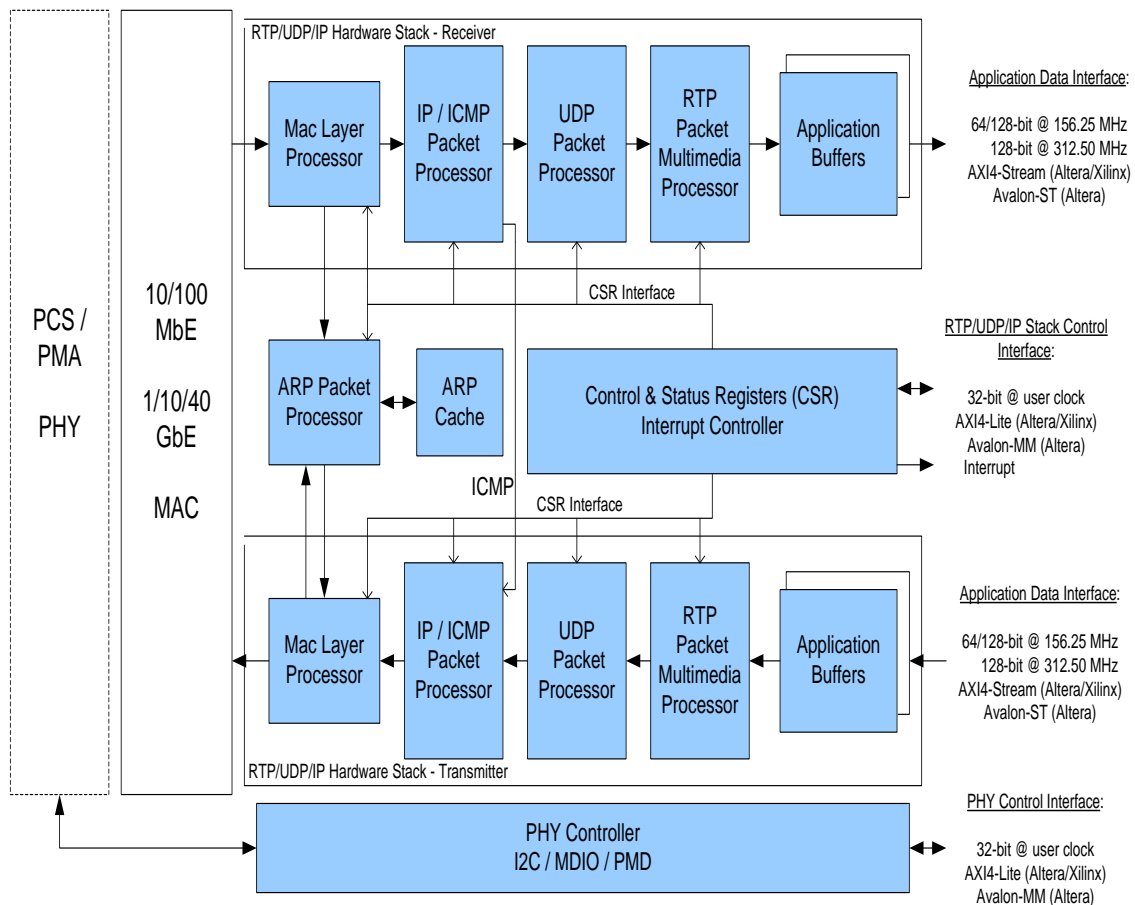


Figure 1: DB-RTP-UDP-IP-AV – RTP/UDP/IP Hardware Stack for Audio/Video Applications

Features

- 10/100 MbE as well as 10/40 Gb wire-line performance with ultra-low latency of Audio/Video encapsulated within an IP/UDP/RTP packet
- Address Resolution Protocol (ARP) Packet Processor (client/server) with 4-16 entry ARP cache
- Internet Protocol (IP) Packet Processor:
 - IPv4 and IPv6 (optional) & ICMP (Internet Control Message Protocol) Protocol
 - IP header checksum generator (transmitter) & check (receiver), user-selectable Maximum Transmission Unit (MTU), Unicast, Broadcast & Multicast Packet support
 - Compliance with IETF IPv4/IPv6 RFCs
- User Datagram Protocol (UDP) Packet Processor:
 - Support for up to 256 UDP Ports
 - UDP header checksum generator (transmitter) & check (receiver)
 - Compliance with IETF UDP RFCs
- Real Time Transport Protocol (RTP) Packet Processor
 - Encapsulates (transmitter) /Decapsulates (receiver) H.264/NAL streams to RTP packets
 - Compliance with IETF RTP RFCs
- High Speed Data Interface to user Host Application:
 - 10 GbE: 64-bit @ 156.25 MHz AXI4-Stream or Avalon-ST
 - 40 GbE: 128-bit @ 312.50 MHz AXI4-Stream or Avalon-ST
- Host set-up & control via Control & Status Registers and Interrupt Controller
 - 32-bit @ user clock rate AXI4-Lite or Avalon-MM
 - Optional hardwired setup
- Pipeline, High Clock Rate, Low Latency architecture & design
- Fully-synchronous, synthesizable RTL Verilog SoC IP core

Customer Evaluation

Digital Blocks offers a variety of methods for prospective customers to evaluate the RTP/UDP/IP Protocol Hardware Stack SoC IP Core. Please contact Digital Blocks for additional information.

Deliverables

The DB-RTP-UDP-IP-AV IP Core is available in synthesizable RTL Verilog or a technology-specific netlist for FPGAs, along with Synopsys Design Constraints, a simulation test bench with expected results, datasheet, and user manual.

Ordering Information

Please contact Digital Blocks for additional technical, pricing, evaluation, and support information.

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