General Description

The Digital Blocks DB-SPI-M-AMBA is a Serial Peripheral Interface (SPI) Controller Verilog IP Core supporting only Master SPI Bus transfers (both Full Duplex and Half Duplex). The DB-SPI-M contains an AMBA AXI, AHB, or APB Bus Interface for interfacing a microprocessor to external SPI Slave devices.

The DB-SPI-M contains Transmit/Receive FIFOs and Finite State Machine control with status & interrupt capability to fully off-load from the microprocessor the transfer of data over the SPI Bus. Optionally, the user can transfer transmitted or received data from the SPI Bus to user memory via an optional DMA Controller.

The DB-SPI-M targets ASIC / ASSP / FPGA integrated circuits, where typically, the microprocessor is an ARM processor, but can be any embedded processor. Figure 1 depicts the system view of the DB-SPI-M Controller IP Core embedded within an integrated circuit device.

The DB-SPI-M offers a Microprocessor a SPI Master only function in a smaller VLSI footprint than the DB-SPI-MS Master/Slave version.

Figure 1: DB-SPI-M Controller – System Diagram
Features

- Master SPI Modes
- Half Duplex / Full Duplex Transfers – Simultaneous Transmit & Receive
- Four Signal Interface:
  - MO - Master Output (Data)
  - MI - Master Input (Data)
  - SCK - Serial Clock
  - SS[N:0] - Slave Select
- Up to N=8 Slave Select (SS) Outputs for multiple Slaves on SPI Bus
- Configurable SPI Modes:
  - Standard SPI Mode (1 Data Lane)
  - Dual SPI Mode (2 Data lanes)
  - Quad SPI Mode (4 Data Lanes)
- Programmable SPI Frame Formats:
  - Programmable SPI Frame
  - Programmable inter-frame gap
  - Programmable LSB-first or MSB-first frames
- Configurable FIFO depth for off-loading the SPI transfers from the processor:
  - Separate Transmit / Receive FIFOs
- Three Clock Domain Configuration options
- SCK Clock Generator:
  - Programmable SCK Rate
  - Programmable Clock Phase & Polarity
- Optional DMA Controller for transfers between System Memory & SPI Bus
- Internal interrupts with masking control
- Available AMBA Microprocessor Interfaces:
  - AXI / AHB / APB Buses
  - 8 / 16 / 32 bit Data Interface
- Compliance with ARM AMBA and Freescale / Motorola SPI specifications:
- Fully-synchronous, synthesizable Verilog RTL core, with rising-edge clocking, no gated clocks, and no internal tri-states, for easy integration into FPGA or ASIC design flows.
Digital Blocks, Inc.  

DB-SPI-M-AMBA  
AMBA Buses SPI Controller

**Pin Description**

In addition to either of the AMBA AXI / AHB/ APB Bus interfaces, which include the input CLOCK and RESET signals and the output INTR (interrupt) signal, the SPI interface signals are listed in Table 1.

<table>
<thead>
<tr>
<th>Name</th>
<th>Type</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>MO</td>
<td>Master - Output</td>
<td>Master - Serial Data Output</td>
</tr>
<tr>
<td>MI</td>
<td>Master - Input</td>
<td>Master - Serial Data Input</td>
</tr>
<tr>
<td>SCK</td>
<td>Master - Output</td>
<td>Master – Serial Clk Output</td>
</tr>
<tr>
<td>SS</td>
<td>Master - Output</td>
<td>Master – Slave Select Output</td>
</tr>
</tbody>
</table>

*Table 1: DB-SPI-MS – I/O Pin Description*

**Verification Method**

The DB-SPI-M Controller IP Core contains a test suite with AMBA AXI, AHB, APB Bus functional models that program the DB-SPI-M control & status registers, generates & sends SPI data, monitors the SPI bus protocol, and checks expected results.

The DB-SPI-M Controller IP Core has internally been verified as follows:

- Instantiated within an FPGA, controlled by an ARM processor, and communicating with (1) merchant semiconductor devices containing SPI Master & Slave bus interfaces; and (2) FPGAs/ASICs containing SPI Master / Slave bus interfaces in Customer implementations.

**Ordering Information**

Digital Blocks DB-SPI-M are available as follows:

<table>
<thead>
<tr>
<th>Digital Blocks Number</th>
<th>AMBA Interface</th>
</tr>
</thead>
<tbody>
<tr>
<td>DB-SPI-M-AXI</td>
<td>AXI Interface – Read/Write Channels</td>
</tr>
<tr>
<td>DB-SPI-M-AXI-Lite</td>
<td>AXI Interface – Read/Write Channels (Reduced Signaling)</td>
</tr>
<tr>
<td>DB-SPI-M-AHB</td>
<td>AHB Slave Interface – Read/Write</td>
</tr>
<tr>
<td>DB-SPI-M-APB</td>
<td>APB Slave Interface – Read/Write</td>
</tr>
</tbody>
</table>

**Customer Evaluation**

Digital Blocks offers a variety of methods for prospective customers to evaluate the DB-SPI-M. Please contact Digital Blocks for additional information.
**Deliverables**

The DB-SPI-M is available in synthesizable RTL Verilog or a technology-specific netlist for FPGAs, along with Synopsys Design Constraints, a simulation test bench with expected results, datasheet, and user manual.

The DB-SPI-M comes along with example C code software for controlling Transmit and Receive Transactions in an Eclipse-based ARM Integrated Development Environment (IDE).

**Ordering Information**

Please contact Digital Blocks for additional technical, pricing, evaluation, and support information.

Digital Blocks, Inc.
PO Box 192
587 Rock Rd
Glen Rock, NJ 07452 USA
Phone: +1-201-251-1281
eFax: +1-702-552-1905
info@digitalblocks.com

Copyright © Digital Blocks, Inc. 2008 - 2018, ALL RIGHTS RESERVED

###
Digital Blocks is a registered trademark of Digital Blocks, Inc.
All other trademarks are the property of their respective owners