General Description

The Digital Blocks DB-SPI-S-AMBA-BRIDGE is a Serial Peripheral Interface (SPI) Controller Verilog IP Core supporting only Slave SPI Bus transfers (both Full Duplex and Half Duplex) to/from a AMBA APB, AXI, or AHB Interconnect.

The DB-SPI-S-AMBA-BRIDGE contains dual clock Transmit/Receive FIFOs and Finite State Machine control to process incoming SPI transmit/receive transactions, and a AMBA Master Interface (i.e. APB, AXI, AHB5) to read or write the SPI payload data with respect to the AMBA Interconnect. No processor is required for configuration or control; the DB-SPI-S-AMBA-BRIDGE operates autonomously from reset.

The DB-SPI-S-AMBA-BRIDGE allows for SPI2APB, SPI2AXI, and SPI2AHB transfers, between the SPI bus and registers or memory attached to the AMBA Interconnect.

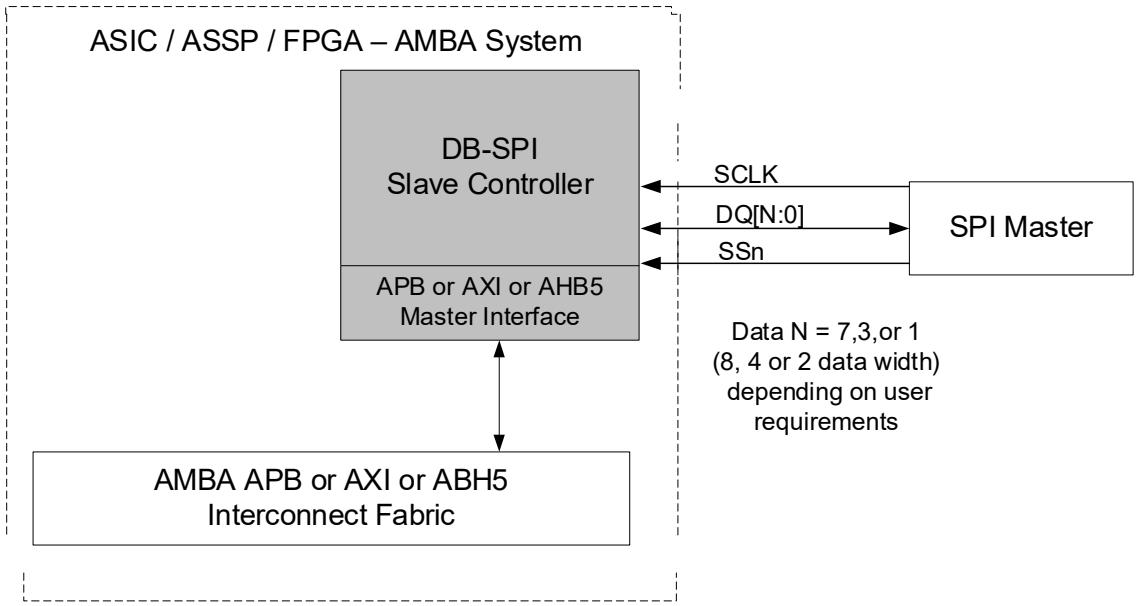

Figure 1: DB-SPI-S-AMBA-BRIDGE Controller – System Diagram

Features

- Three release configurations:
  - SPI Slave to/from APB Master (SPI2APB)
  - SPI Slave to/from AXI Master SPI (AXI)
  - SPI Slave to/from AHB5 Master (SPI2AHB5)
- Signal Interface:
  - DQ-IO[3:0] - Data Input/Output
  - SCK - Serial Clock
  - SSn - Slave Select
- Configurable SPI Modes:
  - Standard SPI Mode (1 Data Lane)
  - Dual SPI Mode (2 Data lanes)
  - Quad SPI Mode (4 Data Lanes)
- Configurable LSB-first or MSB-first Per Word
- Two Clock Domains:
  - AMBA Bus / SCK Clocks
- Separate Transmit / Receive FIFOs:
  - Dual Clock Domains
  - 32-bit Data Width
  - Configurable depth
  - Implemented as Registers (recommended) or SRAM
- Available AMBA Master Interfaces:
  - AXI or APB or AHB
  - 32 bit Data Interface
- Compliance with ARM AXI / APB AMBA specifications:
  - Compliance with AMBA AXI Protocol Specification (V2.0)
  - Compliance with AMBA APB4 Protocol Specification (V2.0)
  - Compliance with ARM AMBA 5 AHB Protocol Specification
- Fully synchronous, synthesizable Verilog RTL core, no gated clocks, and no internal tri-states, for easy integration into FPGA or ASIC design flows.

Verification Method

The DB-SPI-S-AMBA-BRIDGE Controller IP Core contains a test suite with AMBA AXI, AHB, APB Bus functional models that generate & send SPI data, monitors the SPI bus protocol, and checks expected results.

Ordering Information

Digital Blocks DB-SPI-S-AMBA-BRIDGE are available as follows:

Digital Blocks Number	AMBA Interface
DB-SPI-S-AMBA-APB	SPI Slave to/from APB Master
DB-SPI-S-AMBA-AXI	AXI Master version
DB-SPI-S-AMBA-AXI-Lite	AXI-Lite Master version
DB-SPI-S-AMBA-AHB5	AHB5 Master version

Deliverables

The DB-SPI-S-AMBA-BRIDGE is available in synthesizable RTL Verilog or a technology-specific netlist for FPGAs, along with Synopsys Design Constraints, a simulation test bench with expected results, datasheet, and user manual.

Ordering Information

Please contact Digital Blocks for additional technical, pricing, evaluation, and support information.

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