# Digital Blocks
Semiconductor

# DB-SPI-XIP-FLASH-AMBA
SPI XIP Flash Memory Controller

## General Description

The Digital Blocks DB-SPI-XIP-FLASH-AMBA is a Serial Peripheral Interface (SPI) Controller Verilog IP Core supporting access to Single/Dual/Quad/Octal SPI Flash Memory devices by way of Processor Execute-in-Place (XIP).

The DB-SPI-XIP-FLASH-AMBA is a SPI Master Controller targeting SPI NOR/NAND Flash Memories. The DB-SPI-XIP-FLASH-AMBA contains two AMBA Slave Interfaces: the first for Processor configuration or Processor access to the Flash Memory; the second for Processor AMBA Interface for Execute-in-Place (XIP) access to Flash Memory.

Figure 1 depicts the system view of the DB-SPI-XIP-FLASH-AMBA Controller IP Core embedded within an integrated circuit device, with many optional Slave AMBA interface options. The DB-SPI-XIP-FLASH-AMBA contains an AXI or AHB Slave allowing for XIP Memory Read of Flash Memory via the SPI Master Bus, and AXI/AXI-Lite, AHB, or APB Slave Interface for Processor Configuration or Memory Read/Write of Flash Memory.
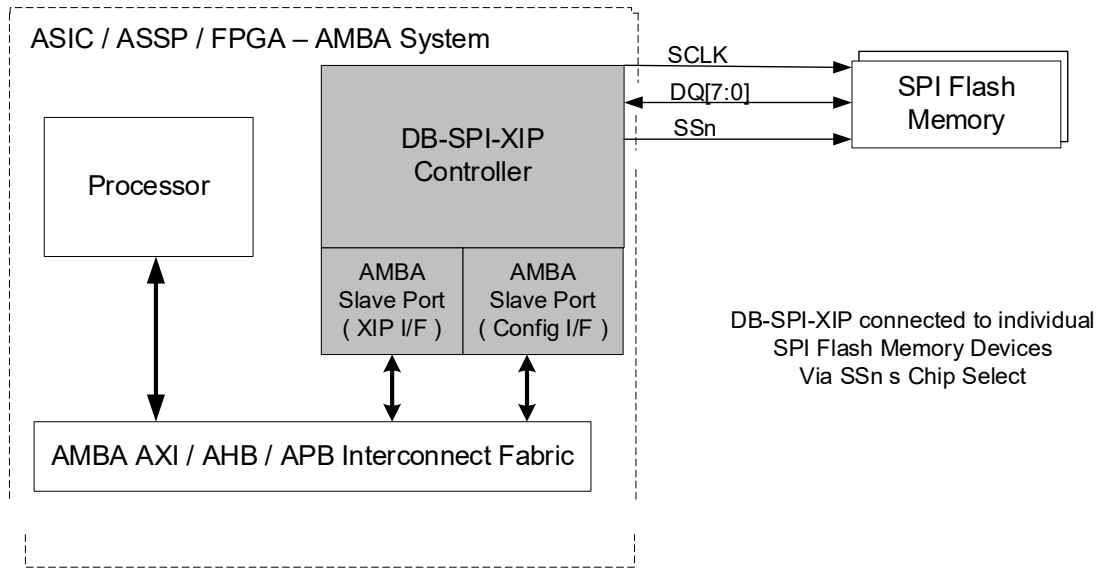


Figure 1: DB-SPI-XIP-FLASH-AMBA Controller – System Diagram

## Features

- Master SPI Controller with two AMBA interfaces to access SPI Flash Memory:
    - AXI/AHB/APB Slave Interface for CPU Configuration & direct read/write of SPI Flash Memory.
    - AXI/AHB Slave Interface for Execute-In-Place (XIP) – accepts AXI/AHB Slave read requests, reads the SPI Flash Memory, and returns the read data
- SPI Flash Memory Support & Interface:
    - Supports Execute-In-Place (XIP), CPU Programmable IO, and DMA. Customers can order with CPU Programmable IO and add any of the additional features as required.
    - Flash Memory from Adesto, Cypress/Spansion, Macronix, Micron, and Winbond
    - Supports SPI Mode0, Mode3 at 200 MHz
    - Up to N=8 Slave Select (SS) Outputs supporting multiple SPI Flash Memory devices. N=16 optional.
    - Configurable SPI Modes:
        - Standard SPI Mode    (1 Data Lane)
        - Dual SPI Mode        (2 Data lanes)
        - Quad SPI Mode        (4 Data Lanes)
        - Octal Mode           (8 Data lanes)
    - Single and Double Transfer Rate (STR/DTR)
    - Programmable SPI Command, Address, Dummy Cycle (latency), and Data lengths
    - Programmable LSB-first or MSB-first Per Word
- Transmit/Receive FIFOs:
    - Dual-Clock designs
    - User configurable depths
- Two Clock Domains:
    - AMBA Bus / SCK Clocks
- Internal interrupts with masking control
- Available AMBA Microprocessor Interfaces:
    - AXI / AHB / APB Buses
    - 8 / 16 / 32 bit Data Interface
- Compliance with ARM AXI4/ AXI3 / AHB / APB AMBA specifications:
    - Compliance with AMBA AXI Protocol Specification (V2.0)
    - Compliance with AMBA APB Protocol Specification (V3.0)
    - Compliance with AMBA Specification (V2.0) - AHB
    - Compliance with AMBA 3 AHB-Lite Protocol (V1.0)
- Compliance with ARM AMBA and Freescale / Motorola SPI specifications:

- Fully-synchronous, synthesizable Verilog RTL core, with rising-edge clocking, no gated clocks, and no internal tri-states, for easy integration into FPGA or ASIC design flows.

## Pin Description

In addition to the two Slave AMBA Interfaces, which include the input AMBA CLOCK and RESET signals and the output INTR (interrupt) signal, the SPI interface signals are listed in Table 1.

| Name | I/O | Description |
|---|---|---|
| **SPI Bus Interface – Master – 4 Data lanes - Bidirectional** | | |
| **DQ/IO[N:0]**<br><br>N=1,2,4,8 option | I/O | **Data Input/Output**– SPI Master bidirectional serial data. SPI Flash Memory pins refer to these as DQ or IO. |
| **SCKO** | O | **Serial Clock Output** – Serial clock output |
| **SSO[N:0]** | O | **Slave Select Output** – Slave Select output.  N can be up to 8 for multiple Flash Memory devices |

**Table 1: DB-SPI-XIP-FLASH-AMBA – I/O Pin Description**

## Verification Method

The DB-SPI-XIP-FLASH-AMBA Controller IP Core contains a test suite with AMBA AXI, AHB, APB Bus functional models that program the DB-SPI-XIP-FLASH-AMBA control & status registers, generates & sends SPI data, tests for XIP, monitors the SPI bus protocol, and checks expected results. SPI Flash Memory models are used in the verification suite.

## Customer Evaluation

Digital Blocks offers a variety of methods for prospective customers to evaluate the DB-DB-SPI-XIP-FLASH-AMBA. Please contact Digital Blocks for additional information.

## Deliverables

The DB-SPI-XIP-FLASH-AMBA is available in synthesizable RTL Verilog or a technology-specific netlist for FPGAs, along with Synopsys Design Constraints, a simulation test bench with expected results, datasheet, and user manual.

## Ordering Information

Please contact Digital Blocks for additional technical, pricing, evaluation, and support information.

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