General Description

The Digital Blocks DB-UDP-IP-100GbE-AMBA is a UDP/IP Hardware Stack / UDP Off-load Engine (UOE) with low latency, high-performance targeting 100 GbE network links. The DB-UDP-IP is a Verilog SoC IP Core targeting Intel/Altera and Xilinx FPGAs and ASIC/ASSP devices.

Figure 1 depicts the UDP/IP Hardware Stack SoC IP Core embedded within an Altera / Xilinx FPGA device, connected on one side to a 100 GbE Ethernet MAC, and on the other side to the user application within the FPGA (i.e. either the FPGA logic fabric or embedded host processor).

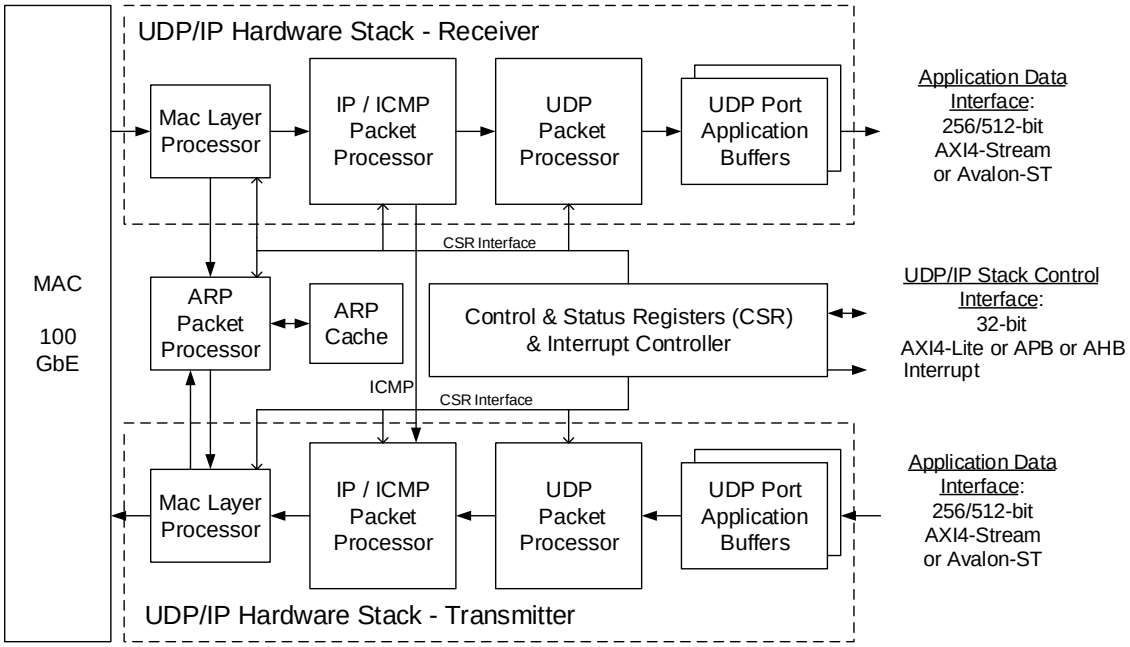

Figure 1: DB-UDP-IP-100GbE-AMBA - Verilog SoC IP Core

Features

- 100 GbE network links
- Low latency, high-performance wire-line performance
- Internet Protocol (IP) Packet Processor:
    - IP & ICMP (Internet Control Message Protocol) Protocol
    - Host IP address filter, IP header checksum check & generator, user-selectable Maximum Transmission Unit (MTU), Unicast & Multicast Packet support
    - Compliance with IETF IPv4/IPv6 RFCs
- User Datagram Protocol (UDP) Packet Processor:
    - Support for up to 256 UDP Ports
    - UDP header checksum check & generator
    - Compliance with IETF UDP RFCs
- Address Resolution Protocol (ARP) Packet Processor (client/server) with 4-16 entry ARP cache
- VLAN Support, DHCP, IGMP, Jumb Frames
- Interface to Intel/Altera (Avalon-ST) & Xilinx & Synopsys 100G MAC
- High Speed Data Interface to user Host Application:
    - 256-bit / 512-bit AXI4-Stream
- Host set-up & control via Control & Status Registers and Interrupt Controller
    - 32-bit AXI4-Lite or APB or AHB
- Pipeline, High Clock Rate, Low Latency architecture & design
- Fully-synchronous, synthesizable RTL Verilog SoC IP core

Design Services

The Digital Blocks offers design services incorporating the UDP/IP Hardware Stack / UDP Off-load Engine (UOE) SoC IP Core targeting Xilinx or Intel/Altera FPGAs. Digital Blocks offers customization features, per customer requirements. Please contact Digital Blocks for additional information.

Customer Evaluation

Digital Blocks offers a variety of methods for prospective customers to evaluate the UDP/IP Hardware Stack UDP Off-load Engine (UOE) SoC IP Core. Please contact Digital Blocks for additional information.

Deliverables

The DB-UDP-IP IP Core is available in synthesizable RTL Verilog or a technology-specific netlist for FPGAs, along with Synopsys Design Constraints, a simulation test bench with expected results, datasheet, and user manual.

Ordering Information

Please contact Digital Blocks for additional technical, pricing, evaluation, and support information.

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