

General Description

The Digital Blocks DB-eSPI-Controller-AMBA is a fully compliant Intel Enhanced Serial Peripheral Interface (eSPI) Base Specification Revision 1.6 (March 2025) **eSPI-Controller** SystemVerilog RTL IP Core, with backward-compatible standard SPI Master mode for legacy SPI peripherals. It contains an AMBA AXI, AHB, or APB Bus Interface for connecting a host microprocessor to one or more external eSPI Targets or legacy SPI Slave devices.

As an eSPI Controller, the DB-eSPI-Controller-AMBA initiates all bus transactions. It issues `PUT_*` commands to write to Target peripherals (memory writes, virtual wires, Out-of-Band messages, flash requests) and `GET_*` commands to retrieve responses, status, and read data from the Target. The IP fully off-loads packet framing, CRC-8 generation and checking, channel arbitration, and response-code decoding from the host microprocessor.

The DB-eSPI-Controller-AMBA contains independent dual-clock Transmit and Receive FIFOs and multiple Finite State Machines with comprehensive status and interrupt capability. Optionally, a DMA Controller can transfer data between user memory and the eSPI / SPI Bus.

The DB-eSPI-Controller targets ASIC / ASSP / FPGA integrated circuits, where typically the host processor is an Intel or ARM or RISC-V processor, but any embedded processor is supported. Figure 1 depicts the system view of the DB-eSPI-Controller IP Core embedded within a host SoC, communicating with one or more external eSPI Targets and / or legacy SPI Slave devices on the shared bus.

Separate Digital Blocks **DB-eSPI-Target-AMBA** for the Target side of an eSPI link and combination **DB-eSPI-Controller-Target-AMBA** releases are available.

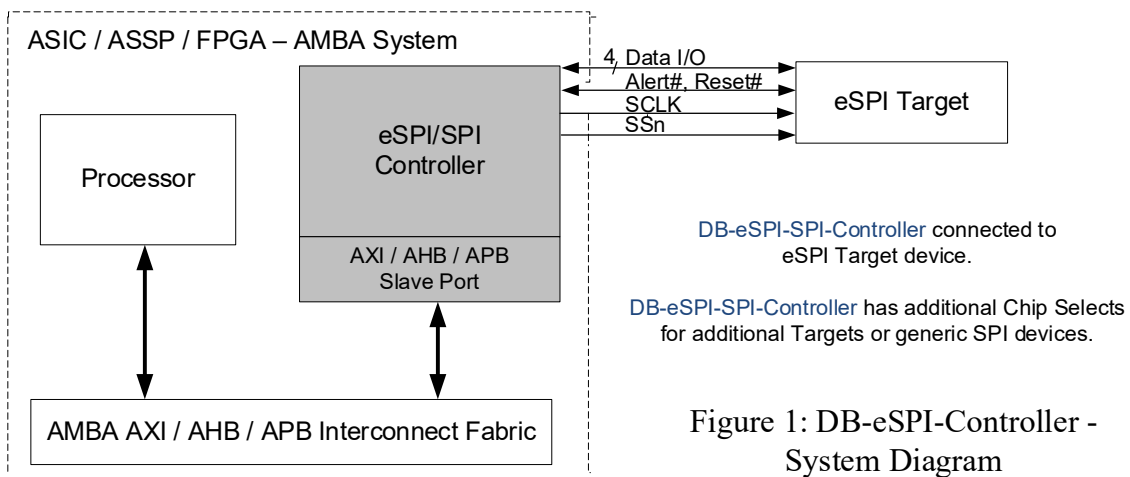


Figure 1: DB-eSPI-Controller - System Diagram

Features – DB-eSPI-Controller-Target

The DB-eSPI-Controller-AMBA is a fully compliant Intel Enhanced Serial Peripheral Interface (eSPI) Base Specification Rev. 1.6 (March 2025) Controller IP core, with backward-compatible standard SPI Master mode and an AMBA APB / AHB / AXI4-Lite host-side interface.

Standards & Compliance

- Full compliance to **eSPI Base Specification Rev. 1.6, Controller** function (Intel document 841685)
- Supports all four eSPI channels — **Ch 0 Peripheral, Ch 1 Virtual Wire, Ch 2 Out-of-Band Message, Ch 3 Flash Access**
- Channel 3 Flash supports both **CAFS** (Controller-Attached Flash Sharing) and **TAFS** (Target-Attached Flash Sharing) modes
- Backward-compatible **standard SPI Master** modes for legacy SPI peripherals

Operating Modes & Throughput

- Selectable per-transfer I/O lane width: **Single (x1), Dual (x2), or Quad (x4)**
- **Full-duplex** eSPI transfers — Command Phase immediately followed by Response Phase on the shared bus
- Programmable channel maximum payload size: 64 / 128 / **256 bytes** per packet
- Up to **64 Virtual Wire groups** supported on Channel 1 (eSPI 1.6 maximum)
- Software-initiated **In-Band Reset** generation to external Targets (eSPI 1.6 §8.3.2)

eSPI Sideband Signals

- **RESET#** — Controller-driven output to external Target(s)
- **ALERT#** — input from external Target(s); generates a host CPU interrupt on assertion

Multi-Target Topology

- **eSPI-Controller** can drive up to **8 external eSPI Targets** on the shared bus (contact Digital Blocks for greater fan-out)
- Per-Target chip-select (Slave Select) outputs for individual Target addressing

Bus & Clocking

- AMBA **APB / AHB / AXI4-Lite slave** interface for register and FIFO access
- Independent **APB clock** and **SCK clock** domains; safe CDC via Gray-coded pointer synchronizers throughout
- Programmable SCK divider; SCK driven from the APB clock or an external clock pin
- Async-assert / sync-deassert reset synchronization on the SCK domain

FIFO Architecture

- Independent **dual-clock asynchronous TX and RX FIFOs**, default **256 bytes each** (parameterizable 4 – 4096 B via *_FIFO_ADDRSIZE)
- Software-readable byte counts and programmable almost-empty / almost-full thresholds per FIFO
- WAIT-State (0x0F) byte filtering on the RX-FIFO write path during the Response Phase

Data Integrity & Protocol Error Handling

- **CRC-8** generator on transmit; CRC-8 checker on receive
- Response-code decoder — host interrupted on Target-reported FATAL_ERROR, NON_FATAL_ERROR, DEFER, or unexpected response
- Per-channel AVAIL / FREE queue-state tracking via the Target's Status bytes
- Programmable Wait-State Response handling (eSPI WSR)

Interrupts

- Single combined Interrupt output with per-source mask, status, and vector registers
- Sources: TX almost-empty, RX almost-full, TX/RX overrun & underrun, master transfer complete, command/response error, external **ALERT#** (Controller mode)

Synthesis & Implementation

- Selectable FIFO memory style — inferred RAM for FPGA Block-RAM / LUTRAM, or register-based for ASIC register-file
- Scan-test ready; clean lint and CDC results
- Validated on **Synopsys Design Compiler** (ASIC) and FPGA flows (**Xilinx Vivado**, **Intel Quartus**)

Features - DB-SPI-MS Controller

- **Standard SPI Master** mode for backward compatibility with legacy SPI Slave peripherals
- **Half-Duplex / Full-Duplex** transfers (simultaneous Transmit & Receive in FD mode)
- Four-signal SPI interface: **MOSI, MISO, SCK, SS[N-1:0]**
- Up to **N = 8 Slave Select outputs** for multiple SPI Slaves on the bus
- Programmable SPI frame formats
- Programmable LSB-first or MSB-first byte order, per word
- Two clock domains: AMBA Bus clock and SCK clock
- Independent dual-clock Transmit / Receive FIFOs — 8-bit data width, configurable depth 4 – 256 bytes, implemented as registers or SRAM
- Optional DMA Controller for memory ↔ SPI Bus transfers
- Internal interrupts with masking control
- Available AMBA / Avalon Microprocessor Interfaces:
 - AXI / AHB / APB / Avalon Buses
 - 8-bit / 32-bit Data Interface
- Fully-synchronous, synthesizable SystemVerilog RTL core, with rising-edge clocking, no gated clocks, and no internal tri-states, for easy integration into FPGA or ASIC design flows.

Verification Method

The DB-eSPI-Controller-AMBA IP Core ships with a comprehensive test suite. AMBA AXI / AHB / APB Bus-functional models program the Controller's control and status registers, generate and send eSPI / SPI commands, monitor the bus protocol on the wire, and check expected Target responses against the eSPI 1.6 specification.

Coverage includes all four eSPI channels (Peripheral, Virtual Wire, OOB Message, Flash Access in both CAFS and TAFS modes), all I/O lane widths (x1, x2, x4), and end-to-end error scenarios.

Deliverables

The DB-eSPI-Controller-AMBA is available in synthesizable SystemVerilog RTL or a technology-specific netlist for FPGAs, along with a simulation testbench with expected results, integration guide, C code bare metal & linux driver, and Technical Reference Manual.

Ordering Information

Digital Blocks, Inc.

DB-eSPI-Controller-AMBA
AMBA Bus Host to eSPI Controller

Please contact Digital Blocks for additional technical, pricing, evaluation, and support information.

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