DB-eSPI-Controller-Target AMBA
AMBA Bus Host to eSPI Controller

General Description

The Digital Blocks DB-eSPI-Controller-Target-AMBA is a fully compliant Intel Enhanced Serial Peripheral Interface (eSPI) Base Specification Revision 1.5 (May 2022) **Controller and Target** SystemVerilog RTL IP Core, with backward-compatible standard SPI Master and Slave modes for legacy SPI peripherals. The same RTL is configurable at integration time as an eSPI Controller, an eSPI Target, or a combined Controller-Target instance, with an AMBA AXI, AHB, or APB Bus Interface for connecting a host or local microprocessor to the eSPI bus.

In **Controller** role, the IP initiates all bus transactions: it issues PUT_* commands to write to Target peripherals (memory writes, virtual wires, Out-of-Band messages, flash requests) and GET_* commands to retrieve responses, status, and read data; it decodes Target response codes; and it can fan out to up to 8 external eSPI Targets on the shared bus.

In **Target** role, the IP responds to Controller commands, generates FATAL_ERROR / NON_FATAL_ERROR / DEFER / ACCEPT responses per eSPI 1.5, manages per-channel AVAIL / FREE queue-status bits, and signals back to the Controller via the **ALERT#** sideband on local interrupt events.

The IP fully off-loads packet framing, CRC-8 generation and checking, channel arbitration, response-code decoding (Controller) or generation (Target), and queue-status tracking from the host microprocessor. It contains independent dual-clock Transmit and Receive FIFOs and multiple Finite State Machines with comprehensive status and interrupt capability. Optionally, a DMA Controller can transfer data between user memory and the eSPI / SPI Bus.

The DB-eSPI-Controller-Target targets ASIC / ASSP / FPGA integrated circuits, where typically the host or local processor is an Intel, ARM, or RISC-V processor, but any embedded processor is supported. Figure 1 depicts the system view of the DB-eSPI-Controller-Target IP Core embedded within an SoC, communicating over the eSPI bus with peer eSPI Targets, Controllers, and / or legacy SPI Master/Slave devices.

Separate Digital Blocks DB-eSPI-Controller-AMBA (Controller only) and DB-eSPI-Target-AMBA (Target only) releases are also available.

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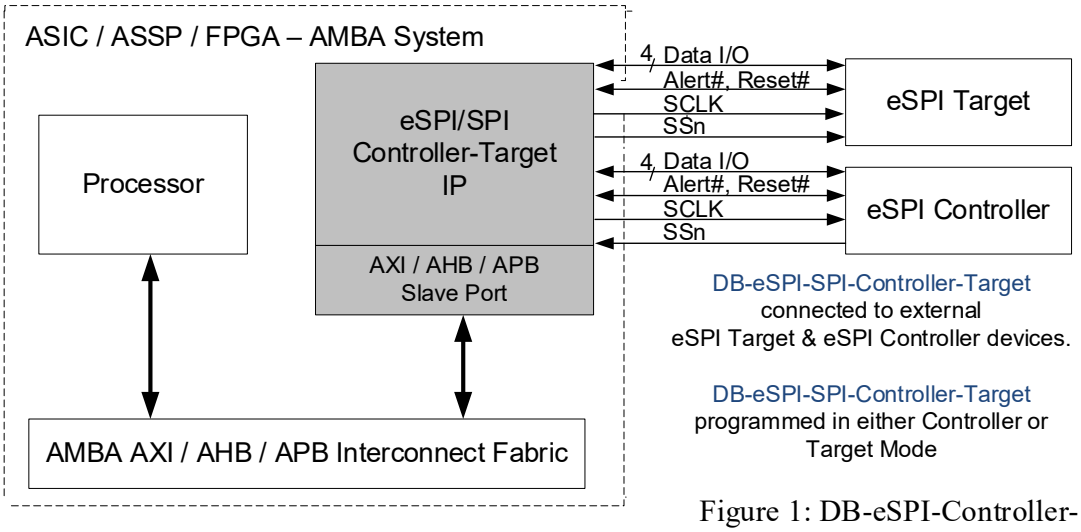

Figure 1: DB-eSPI-Controller-Target - System Diagram

Features – DB-eSPI-Controller-Target

The DB-eSPI-Controller-Target-AMBA is a fully compliant Intel eSPI Base Specification Rev. 1.5 (May 2022) Controller and Target IP core with backward-compatible standard SPI Master and Slave modes and an AMBA APB / AHB / AXI4-Lite host-side interface.

Standards & Compliance

- Full compliance to **eSPI Base Specification Rev. 1.5**, both Controller and Target functions (Intel document 327432-005)
- Supports all four eSPI channels — **Ch 0 Peripheral**, **Ch 1 Virtual Wire**, **Ch 2 Out-of-Band Message**, **Ch 3 Flash Access**
- Channel 3 Flash supports both **CAFS** (Controller-Attached Flash Sharing) and **TAFS** (Target-Attached Flash Sharing) modes
- Backward-compatible **standard SPI Master and Slave** modes for legacy SPI peripherals

Operating Modes & Throughput

- Configurable as **eSPI Controller**, **eSPI Target**, or **combined Controller + Target** from a single RTL (either Controller or Target programmed active)
- Selectable per-transfer I/O lane width: **Single (x1), Dual (x2), or Quad (x4)**
- **Full-duplex** eSPI transfers — Command Phase immediately followed by Response Phase on the shared bus
- Programmable channel maximum payload size: 64 / 128 / **256 bytes** per packet
- Up to **64 Virtual Wire groups** supported on Channel 1 (eSPI 1.5 maximum)
- **In-Band Reset (IBR)** generation (Controller role) and detection with interrupt (Target role) per eSPI 1.5 §3.5

eSPI Sideband Signals

- **RESET#** — driven by the Controller, received by the Target; I/O direction programmable to support either role
- **ALERT#** — driven by the Target on local event, received by the Controller and generates a host CPU interrupt on assertion

Multi-Target Topology

- Controller role: drives up to **8 external eSPI Targets** on the shared bus (contact Digital Blocks for greater fan-out)
- Target role: responds to a single bus Controller per eSPI 1.5
- Per-Target chip-select (Slave Select) outputs for individual Target addressing

Bus & Clocking

- AMBA **APB / AHB / AXI4-Lite slave** interface for register and FIFO access on both Controller and Target sides
- Independent **APB clock** and **SCK clock** domains; safe CDC via Gray-coded pointer synchronizers throughout
- Programmable SCK divider; SCK driven from the APB clock or external clock pin (Controller drives, Target receives)
- Async-assert / sync-deassert reset synchronization on the SCK domain

FIFO Architecture

- Independent **dual-clock asynchronous TX and RX FIFOs**, default **256 bytes each** (parameterizable 4 – 4096 B via `*_FIFO_ADDRSIZE`)
- Software-readable byte counts and programmable almost-empty / almost-full thresholds per FIFO
- Controller WAIT-State (`0x0F`) byte filtering on the RX-FIFO write path during the Response Phase
- Recommended buffer sizes for Maximum-GCC operation across all four channels documented in the TRM (Section "FIFO Sizing — eSPI Target")

Data Integrity & Protocol Error Handling

- **CRC-8** generator on transmit; CRC-8 checker on receive
- **Target role**: hardware-generated `FATAL_ERROR` response on RX CRC mismatch, `GET_*` with channel `AVAIL = 0`, `PUT_NP` with NP RX `FREE = 0`, `PUT_FLASH_C` (CAFS) or `PUT_FLASH_NP` (TAFS) with Flash RX `FREE = 0`
- **Target role**: programmable WAIT-STATE response; hardware-generated `DEFER` on WAIT-State timeout; `ACCEPT` with optional channel-specific modifier
- **Controller role**: response-code decoder — host interrupted on Target-reported `FATAL_ERROR`, `NON_FATAL_ERROR`, `DEFER`, or unexpected response
- Per-channel `AVAIL` / `FREE` queue-state tracking via the Target's Status bytes

Interrupts

- Single combined Interrupt output with per-source mask, status, and vector registers
- Sources (role-dependent): TX almost-empty, RX almost-full, TX/RX overrun & underrun, master / slave transfer complete (MTC / STC), command / response error, CRC error, external **ALERT#** (Controller role), **In-Band Reset (IBR) detected** (Target role)

Synthesis & Implementation

- Selectable FIFO memory style — inferred RAM for FPGA Block-RAM / LUTRAM, or register-based for ASIC register-file
- Scan-test ready; clean lint and CDC results

- Validated on **Synopsys Design Compiler** (ASIC) and FPGA flows (**Xilinx Vivado**, **Intel Quartus**)

Features - DB-SPI-MS (Legacy SPI Master and Slave Modes)

- **Standard SPI Master and Slave** modes for backward compatibility with legacy SPI peripherals
- **Half-Duplex / Full-Duplex** transfers (simultaneous Transmit & Receive in FD mode)
- Four-signal SPI interface: **MOSI**, **MISO**, **SCK**, **SS[N-1:0]**
- Up to **N = 8 Slave Select outputs** for multiple SPI Slaves on the bus (Master mode)
- Programmable SPI frame formats
- Programmable LSB-first or MSB-first byte order, per word
- Two clock domains: AMBA Bus clock and SCK clock
- Independent dual-clock Transmit / Receive FIFOs — 8-bit data width, configurable depth 4 – 256 bytes, implemented as registers or SRAM
- Optional DMA Controller for memory ↔ SPI Bus transfers
- Internal interrupts with masking control
- Available AMBA / Avalon Microprocessor Interfaces: AXI / AHB / APB / Avalon Buses
- 8-bit / 32-bit Data Interface
- Fully-synchronous, synthesizable SystemVerilog RTL core, with rising-edge clocking, no gated clocks, and no internal tri-states, for easy integration into FPGA or ASIC design flows.

Verification Method

The DB-eSPI-Controller-Target-AMBA IP Core ships with a comprehensive test suite covering **both** Controller and Target roles. The testbench instantiates two IP instances on the same eSPI bus — one configured as Controller, one as Target — and exercises end-to-end command, response, and error sequences. AMBA AXI / AHB / APB Bus-functional models program both sides' control and status registers, the testbench monitors the bus protocol on the wire, and expected responses are checked against the eSPI 1.5 specification.

Coverage includes all four eSPI channels (Peripheral, Virtual Wire, OOB Message, Flash Access in both CAFS and TAFS modes), all I/O lane widths (x1, x2, x4), and end-to-end error scenarios (CRC mismatch, FATAL_ERROR generation and decode, DEFER recovery, In-Band Reset generation and detection including ISR propagation).

Deliverables

The DB-eSPI-Controller-Target-AMBA is available in synthesizable SystemVerilog RTL or a technology-specific netlist for FPGAs, along with a simulation testbench with

expected results, integration guide, C-code bare-metal and Linux driver, and Technical Reference Manual.

Ordering Information

Please contact Digital Blocks for additional technical, pricing, evaluation, and support information.

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