General Description

The Digital Blocks DB-eSPI-MS-AMBA is a Serial Peripheral Interface (SPI) Controller Verilog IP Core supporting the addition of Enhanced SPI (eSPI) bus transfers to the standard SPI Master/Slave Controller. The DB-eSPI-MS contains an AMBA AXI, AHB, or APB Bus Interface for interfacing a microprocessor to external SPI Master/Slave devices.

The DB-eSPI-MS contains Transmit/Receive FIFOs and Finite State Machine control with status & interrupt capability to fully off-load from the microprocessor the transfer of data over the SPI Bus. Optionally, the user can transfer transmitted or received data from the SPI Bus to user memory via an optional DMA Controller.

The DB-eSPI-MS targets ASIC / ASSP / FPGA integrated circuits, where typically, the microprocessor is an ARM processor, but can be any embedded processor. Figure 1 depicts the system view of the DB-eSPI-MS Controller IP Core embedded within an integrated circuit device.

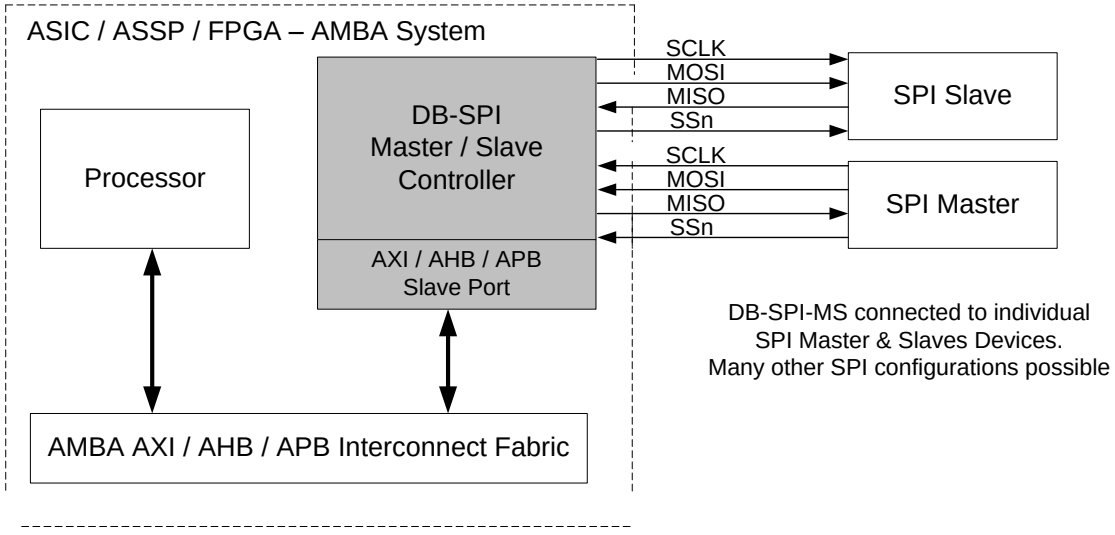

Figure 1: DB-SPI-MS Controller – System Diagram

Features

- Master and Slave SPI Modes
- Half Duplex / Full Duplex Transfers – Simultaneous Transmit & Receive
- Four Signal Interface (1-lane, 4-wire Interface):
  - MOSI - Master Output, Slave Input (Data)
  - MISO - Master Input, Slave Output (Data)
  - SCK - Serial Clock
  - SS[N:0] - Slave Select
- Up to N=8 Slave Select (SS) Outputs for multiple Slaves on SPI Bus
- Configurable SPI Modes (Optional):
  - Standard SPI Mode (1 Data Lane)
  - Dual SPI Mode (2 Data lanes)
  - Quad SPI Mode (4 Data Lanes)
- 3-wire SPI Interface (Optional)
- Programmable SPI Frame Formats:
  - Programmable Words-Per-Frame (1 to Full Depth of FIFO)
  - Programmable LSB-first or MSB-first frames
- Two Clock Domains:
  - AMBA Bus / SCK Clocks
- SCK Clock Generator - Master Mode (Optional):
  - Programmable SCK Rate
  - Programmable Clock Phase & Polarity
- Configurable FIFO depth for off-loading the SPI transfers from the processor:
  - Separate Transmit / Receive FIFOs
- Optional DMA Controller for transfers between User Memory & SPI Bus
- Internal interrupts with masking control
- Available AMBA Microprocessor Interfaces:
  - AXI / AHB / APB Buses
  - 8 / 16 / 32 bit Data Interface
- DB-eSPI-MS Controller IP Core contains extensions to support the Enhanced Serial Peripheral Interface (eSPI), for eSPI Master, conforming to the Interface Base Specification, January 2016, Revision 1.0.
- Compliance with ARM AMBA and Freescale / Motorola SPI specifications:
- Fully-synchronous, synthesizable Verilog RTL core, with rising-edge clocking, no gated clocks, and no internal tri-states, for easy integration into FPGA or ASIC design flows.

Pin Description

In addition to either of the AMBA AXI / AHB/ APB Bus interfaces, which include the input CLOCK and RESET signals and the output INTR (interrupt) signal, the SPI interface signals are listed in Table 1.

Name	Type	Description
SPI Bus Interface		
MOSI	Master - Output	Master - Serial Data Output
	Slave - Input	Slave - Serial Data Input
MISO	Master - Input	Master - Serial Data Input
	Slave - Output	Slave - Serial Data Output
SCLK	Master - Output	Master - Serial Clk Output
	Slave - Input	Slave - Serial Clk Input
SS	Master - Output	Master – Slave Select Output
	Slave - Input	Slave - Serial Select Input

Table 1: DB-SPI-MS – I/O Pin Description – 1-Lane, 4-wire Interface

Verification Method

The DB-eSPI-MS Controller IP Core contains a test suite with AMBA AXI, AHB, APB Bus functional models that program the DB-eSPI-MS control & status registers, generates & sends SPI data, monitors the SPI bus protocol, and checks expected results.

The DB-eSPI-MS Controller IP Core has internally been verified as follows:

- Instantiated within an FPGA, controlled by an ARM processor, and communicating with (1) merchant semiconductor devices containing SPI Master & Slave bus interfaces and eSPI Slave bus interface; and (2) FPGAs/ASICs containing SPI Master / Slave bus interfaces in Customer implementations.

Ordering Information

Digital Blocks DB-SPI-MS are available as follows:

Digital Blocks Number	AMBA Interface
DB-SPI-MS-AXI	AXI Interface – Read/Write Channels
DB-SPI-MS-AXI-Lite	AXI Interface – Read/Write Channels (Reduced Signaling)
DB-SPI-MS-AHB	AHB Slave Interface – Read/Write
DB-SPI-MS-APB	APB Slave Interface – Read/Write

Customer Evaluation

Digital Blocks offers a variety of methods for prospective customers to evaluate the DB-eSPI-MS. Please contact Digital Blocks for additional information.

Deliverables

The DB-eSPI-MS is available in synthesizable RTL Verilog or a technology-specific netlist for FPGAs, along with Synopsys Design Constraints, a simulation test bench with expected results, datasheet, and user manual.

The DB-eSPI-MS comes along with example C code software for controlling Transmit and Receive Transactions in an Eclipse-based ARM Integrated Development Environment (IDE).

Ordering Information

Please contact Digital Blocks for additional technical, pricing, evaluation, and support information.

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