General Description

The Digital Blocks DB-eSPI-SPI-MS-AMBA is a Serial Peripheral Interface (SPI) Controller Verilog IP Core supporting the addition of Enhanced SPI (eSPI) bus transfers to the standard SPI Master/Slave Controller. The DB-eSPI-SPI-MS contains an AMBA AXI, AHB, or APB Bus Interface for interfacing a microprocessor to external eSPI or SPI Master/Slave devices.

The DB-eSPI-SPI-MS contains both eSPI and SPI Master and Slave functions. Programming the DB-eSPI-SPI-MS lets it communicate with external eSPI or SPI Master or Slaves.

The DB-eSPI-SPI-MS contains Transmit/Receive FIFOs and multiple Finite State Machine control with status & interrupt capability to fully off-load from the microprocessor the transfer of data over the eSPI/SPI Bus. Optionally, the user can transfer transmitted or received data from the eSPI/SPI Bus to user memory or registers via an optional DMA Controller.

The DB-eSPI-SPI-MS targets ASIC / ASSP / FPGA integrated circuits, where typically, the microprocessor is an ARM or RISC-V processor, but can be any embedded processor. Figure 1 depicts the system view of the DB-eSPI-SPI-MS Controller IP Core embedded within an integrated circuit device.

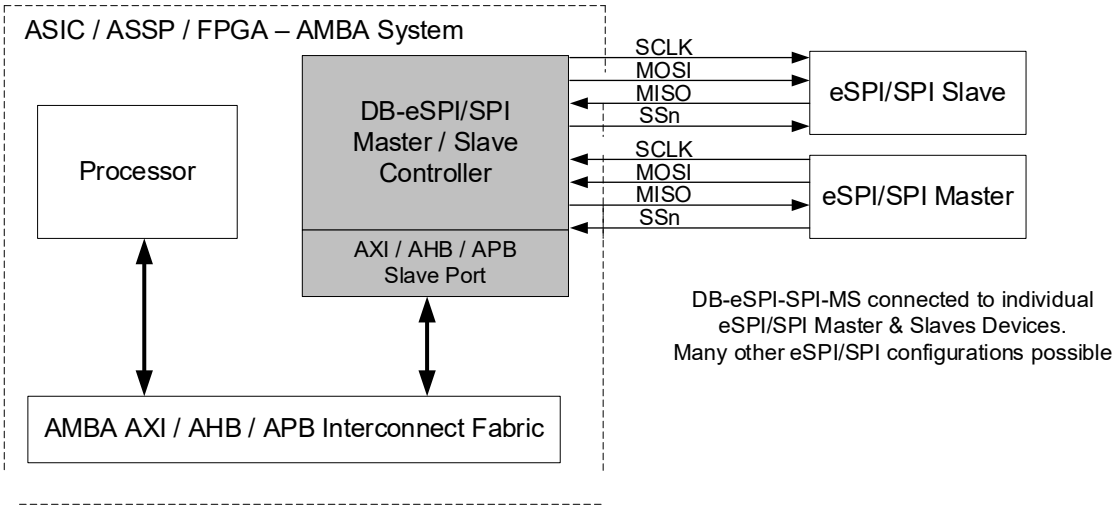

Figure 1: DB-eSPI-SPI-MS Controller – System Diagram

Features – DB-eSPI-MS Controller

- Master & Slave eSPI and standard Master/Slave SPI Modes (see below)
- eSPI Full Duplex Transfers - Command Phase followed by Response Phase
- eSPI Slave supports eSPI Bus Protocol and Transaction and Link Layer requirements
- Additional eSPI Signals to SPI Interface:
    - RESET#
    - ALERT#
- RESET# programmable as input or output
- ALERT# input interrupts CPU
- Support for interface up to 8 eSPI Slaves (Contact Digital Blocks if more needed)
- CRC-8 Generator on Transmit & Checker on Receive
- Compliance to eSPI Master function with Enhanced Serial Peripheral Interface (eSPI), Interface Base Specification, January 2016, Revision 1.0.

Features – DB-SPI-MS Controller

- Master and Slave SPI Modes
- Half Duplex / Full Duplex Transfers – Simultaneous Transmit & Receive
- Original 4 Signal Interface (1 data lane, 4-wire Interface):
    - MOSI - Master Output, Slave Input (Data)
    - MISO - Master Input, Slave Output (Data)
    - SCK - Serial Clock
    - SS[N:0] - Slave Select
- Configurable SPI Modes for 1/2/4/ Data Lanes: (Optional):
    - Standard SPI Mode (1 Data Lane)
    - Dual SPI Mode (2 Data lanes)
    - Quad SPI Mode (4 Data Lanes)
- 3-wire SPI Interface (Optional)
- Up to N=8 Slave Select (SS) Outputs for multiple Slaves on SPI Bus
- Programmable SPI Frame Formats:
    - Programmable Words-Per-Frame (1 to Full Depth of FIFO)
    - Programmable LSB-first or MSB-first frames
- Two Clock Domains:
    - AMBA Bus / SCK Clocks
- SCK Clock Generator - Master Mode (Optional):
    - Programmable SCK Rate
    - Programmable Clock Phase & Polarity
- Configurable FIFO depth for off-loading the SPI transfers from the processor:
    - Separate Transmit / Receive FIFOs

- Optional DMA Controller for transfers between User Memory & SPI Bus
- Internal interrupts with masking control
- Available AMBA Microprocessor Interfaces:
  - AXI / AHB / APB Buses
  - 8 / 16 / 32 bit Data Interface
- Fully-synchronous, synthesizable Verilog RTL core, with rising-edge clocking, no gated clocks, and no internal tri-states, for easy integration into FPGA or ASIC design flows.

Verification Method

The DB-eSPI-SPI-MS Controller IP Core contains a test suite with AMBA AXI, AHB, APB Bus functional models that program the DB-eSPI-SPI-MS control & status registers, generates & sends eSPI or SPI data, monitors the eSPI or SPI bus protocol, and checks expected results.

Customer Evaluation

Digital Blocks offers a variety of methods for prospective customers to evaluate the DB-eSPI-SPI-MS. Please contact Digital Blocks for additional information.

Deliverables

The DB-eSPI-SPI-MS is available in synthesizable RTL Verilog or a technology-specific netlist for FPGAs, along with Synopsys Design Constraints, a simulation test bench with expected results, datasheet, and user manual.

Ordering Information

Please contact Digital Blocks for additional technical, pricing, evaluation, and support information.

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