

### General Description

The Digital Blocks DB-eSPI-Target-AMBA is a fully compliant Intel Enhanced Serial Peripheral Interface (eSPI) Base Specification Revision 1.5 (May 2022) **eSPI-Target** SystemVerilog RTL IP Core, with backward-compatible standard SPI Slave mode for legacy SPI Master hosts. It contains an AMBA AXI, AHB, or APB Bus Interface for connecting a local microprocessor (or memory-mapped subsystem) to an external eSPI Controller.

As an eSPI Target, the DB-eSPI-Target-AMBA responds to `PUT_*` commands from the Controller (memory writes, virtual-wire updates, OOB messages, flash requests) and supplies completion data, status, and read data on `GET_*` commands. The IP fully off-loads packet framing, CRC-8 generation and checking, per-channel queue-status tracking, and response-code generation from the local microprocessor.

The DB-eSPI-Target-AMBA contains independent dual-clock Transmit and Receive FIFOs and multiple Finite State Machines with comprehensive status and interrupt capability. Optionally, a DMA Controller can transfer data between user memory and the eSPI / SPI Bus.

The DB-eSPI-Target targets ASIC / ASSP / FPGA integrated circuits, where typically the local processor is an Intel, ARM, or RISC-V processor, but any embedded processor is supported. Figure 1 depicts the system view of the DB-eSPI-Target IP Core embedded within a Target SoC, communicating with an external eSPI Controller (and / or legacy SPI Master) on the shared bus.

Separate Digital Blocks **DB-eSPI-Controller-AMBA** for the Controller side of an eSPI link and combination **DB-eSPI-Controller-Target-AMBA** releases are available.

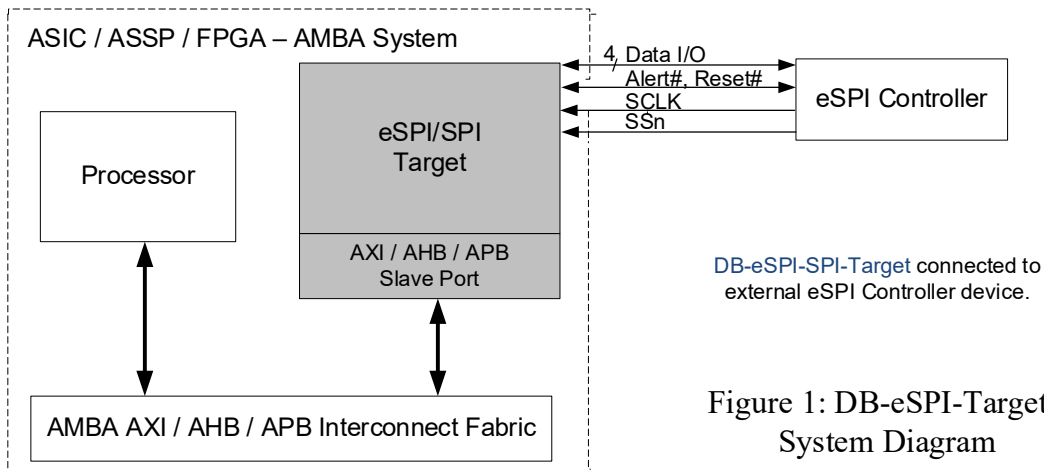


Figure 1: DB-eSPI-Target - System Diagram

## Features – DB-eSPI-Target

The DB-eSPI-Target-AMBA is a fully compliant Intel eSPI Base Specification Rev. 1.5 (May 2022) Target IP core, with backward-compatible standard SPI Slave mode and an AMBA APB / AHB / AXI4-Lite local-side interface.

### Standards & Compliance

- Full compliance to **eSPI Base Specification Rev. 1.5**, Target function (Intel document 327432-005)
- Supports all four eSPI channels — **Ch 0 Peripheral, Ch 1 Virtual Wire, Ch 2 Out-of-Band Message, Ch 3 Flash Access**
- Channel 3 Flash supports both **CAFS** (Controller-Attached Flash Sharing) and **TAFS** (Target-Attached Flash Sharing) modes
- Backward-compatible **standard SPI Slave** mode for legacy SPI Master hosts

### Operating Modes & Throughput

- Selectable per-transfer I/O lane width: **Single (x1), Dual (x2), or Quad (x4)** — accepted from Controller's SET\_CONFIGURATION
- **Full-duplex** eSPI transfers — Command Phase immediately followed by Response Phase on the shared bus
- Programmable channel maximum payload size advertised in GCC / CHxCC capability registers: 64 / 128 / **256 bytes** per packet
- Up to **64 Virtual Wire groups** supported on Channel 1 (eSPI 1.5 maximum)
- **In-Band Reset (IBR) detection** on the bus with local interrupt — restores GCC register (Offset 008h-00Bh) to default state per eSPI 1.5 §3.5

### eSPI Sideband Signals

- **RESET#** — input from the Controller; on assertion, resets all SCK-domain logic and Slave-side configuration (GCC, CHxCC, channel-status). APB-side CSRs (CR1, CR2, ISR, IMR, FIFO thresholds) survive RESET#.
- **ALERT#** — Target-driven output to the Controller, asserted on local interrupt event

### Controller Topology

- Responds to a single bus Controller per eSPI 1.5

### Bus & Clocking

- AMBA **APB / AHB / AXI4-Lite slave** interface for register and FIFO access on the local side
- Independent **local APB clock** and **SCK clock** domains; safe CDC via Gray-coded pointer synchronizers throughout
- SCK is received from the external Controller

- Async-assert / sync-deassert reset synchronization on the SCK domain

### FIFO Architecture

- Independent **dual-clock asynchronous TX and RX FIFOs**, default **256 bytes each** (parameterizable 4 – 4096 B via \*\_FIFO\_ADDRSIZE)
- Software-readable byte counts and programmable almost-empty / almost-full thresholds per FIFO
- Recommended buffer sizes for Maximum-GCC operation across all four channels documented in the TRM (Section "FIFO Sizing — eSPI Target")

### Data Integrity & Protocol Error Handling

- **CRC-8** generator on transmit; CRC-8 checker on receive
- Hardware-generated **FATAL\_ERROR** response on: RX CRC mismatch; GET\_\* with channel TX AVAIL = 0; PUT\_NP with NP RX queue FREE = 0; PUT\_FLASH\_C (CAFS) or PUT\_FLASH\_NP (TAFS) with Flash RX queue FREE = 0
- Programmable **WAIT-STATE** response generation
- Hardware-generated DEFER response on WAIT-State timeout
- ACCEPT response with optional channel-specific modifier

### Interrupts

- Single combined Interrupt output with per-source mask, status, and vector registers  
Sources: TX almost-empty, RX almost-full, TX/RX overrun & underrun, slave transfer complete (STC), command / response error, CRC error, **In-Band Reset (IBR) detected** from Controller

### Synthesis & Implementation

- Selectable FIFO memory style — inferred RAM for FPGA Block-RAM / LUTRAM, or register-based for ASIC register-file
- Scan-test ready; clean lint and CDC results
- Validated on **Synopsys Design Compiler** (ASIC) and FPGA flows (**Xilinx Vivado**, **Intel Quartus**)

## Features - DB-SPI-Slave (Legacy SPI Mode)

- **Standard SPI Slave** mode for backward compatibility with legacy SPI Master hosts
- **Half-Duplex / Full-Duplex** transfers (simultaneous Transmit & Receive in FD mode)
- Four-signal SPI interface: **MOSI, MISO, SCK, SS#**
- Programmable SPI frame formats
- Programmable LSB-first or MSB-first byte order, per word
- Two clock domains: AMBA Bus clock and SCK clock (SCK driven by external Master)
- Independent dual-clock Transmit / Receive FIFOs — 8-bit data width, configurable depth 4 – 256 bytes, implemented as registers or SRAM
- Optional DMA Controller for memory ↔ SPI Bus transfers
- Internal interrupts with masking control
- Available AMBA / Avalon Microprocessor Interfaces: AXI / AHB / APB / Avalon Buses
- 8-bit / 32-bit Data Interface
- Fully-synchronous, synthesizable SystemVerilog RTL core, with rising-edge clocking, no gated clocks, and no internal tri-states, for easy integration into FPGA or ASIC design flows.

## Verification Method

The DB-eSPI-Target-AMBA IP Core ships with a comprehensive test suite. AMBA AXI / AHB / APB Bus-functional models program the Target's control, configuration, and status registers; an eSPI Controller bus-functional model drives commands on the wire; and the testbench monitors expected Target responses (ACCEPT / DEFER / FATALERROR / NONFATAL\_ERROR / WAIT-STATE) against the eSPI 1.5 specification.

Coverage includes all four eSPI channels (Peripheral, Virtual Wire, OOB Message, Flash Access in both CAFS and TAFS modes), all I/O lane widths (x1, x2, x4), and end-to-end error scenarios (CRC mismatch, FATAL\_ERROR generation paths, DEFER recovery, In-Band Reset detection and ISR bit-27 propagation).

## Deliverables

The DB-eSPI-Target-AMBA is available in synthesizable SystemVerilog RTL or a technology-specific netlist for FPGAs, along with a simulation testbench with expected results, integration guide, C-code bare-metal and Linux driver, and Technical Reference Manual.

## Ordering Information

Please contact Digital Blocks for additional technical, pricing, evaluation, and support information.

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