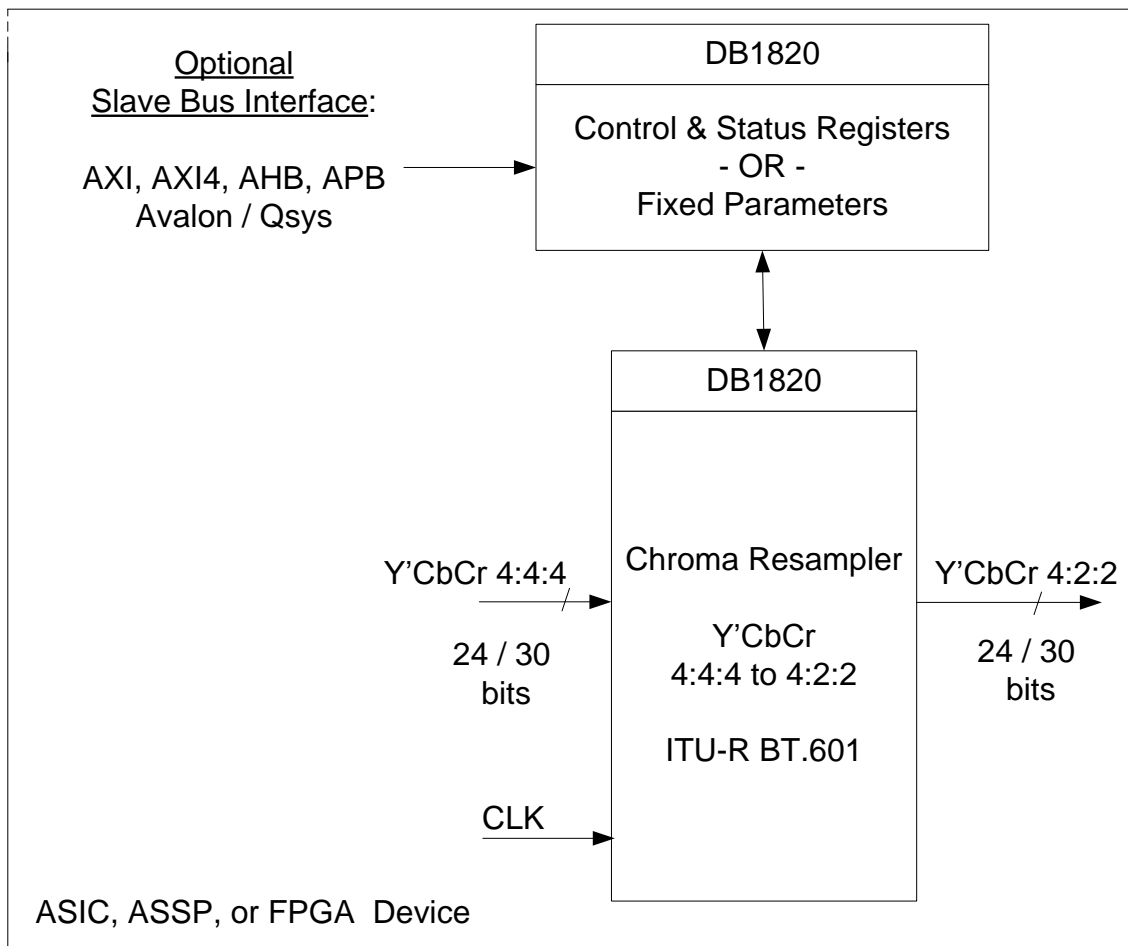


**General Description**

The Digital Blocks DB1820 Chroma Resampler IP Core down converts 4:4:4 Y'CbCr to 4:2:2 Y'CbCr in accordance with the ITU-R BT.601 standard requirements.

Figure 1 depicts the DB1820 Chroma Resampler IP Core embedded within an integrated circuit device. The DB1820 accepts 4:4:4 Y'CbCr digital components and timing control signals and down converts them to 4:2:2 Y'CbCr components. Control & Status, including the down converter's filter coefficients, can be programmed into optional DB1820 registers via a bus interface, or set as non-register fixed parameters at synthesis for a smaller VLSI footprint.



**Figure 1: DB1810 Chroma Resampler**

## Features

- 4:4:4 Y'CbCr and 4:2:2 Y'CbCr input & output components each at 8- or 10-bits, unsigned data type. User selectable at 24- or 30-bit parallel or serial input / output.
- Coefficients are 3-bit fractional data type
- Control signal enable for start-up and blanking period disabling
- After down conversion, each CbCr sample component can be truncated or rounded-up, and saturated or clamped for overflow or underflow, respectively
- Equalization of Y' component and optional delay for display VSYNC, HSYNC, and DE signals
- User optional Slave Bus Interface for programming Control & Status Registers, which includes the down converters coefficients, or fixed parameters set at synthesis
- Member of Digital Blocks' *Video Signal & Image Processing IP Core Family*, which include the following:
  - DB1800 - Standard Definition NTSC/PAL/SECAM Video Sync Separator
  - DB1810 - Color Space Convert
  - DB1820 - Chroma Resampler
  - DB1825 - RGB to Y'CbCr Color Space Convert with 4:4:4 to 4:2:2 Chroma Resampler
  - DB1830 - BT.656 Encoder
  - DB1840 - BT.656 Decoder
  - DB1892 - RGB to CCIR601/656 Encoder
- On-Chip Interconnect Compliance (optional) – Avalon/Qsys, AXI, AXI4, AHB:
  - Avalon Interface Specification (MNL-AVABUSREF-2.0)
  - AMBA AXI Protocol Specification (V1.0)
  - AMBA AXI4 Protocol Specification (V3.0)
  - AMBA AHB Specification 2.0
  - AMBA APB Specification 2.0
- FPGA Integration Support:
  - Altera Quartus II & Qsys / SOPC Integration & NIOS II EDS Reference Design
  - Xilinx ISE Design Suite utilizing AMBA AXI4 & Embedded Development & Software Development Kits
- ASIC / ASSP Design-In Support:
  - Compliance to RTL Design & Coding Standards
  - Digital Blocks Support Services
- Fully-synchronous, pipelined architecture, synthesizable Verilog RTL core

## Pin Description

The DB1820 Chroma Resampler contains optional AMBA bus AXI, AXI4, AHB, APB and Avalon / Qsys bus for processor programming of internal parameters. The DB1820 optionally contains no bus interface with hard-coding of the down converters parameters.

The DB1820 contains the following I/O interface. For information on a bus fabric interface I/O, please contact Digital Blocks.

Name	Type	Description
<b>Input Interface</b>		
CR_PCLK	Input	CR Sample Clock
CR_PRESETN	Input	CR Reset
CR_Y_IN	Input	CR Y' – Luma Component
CR_CB_IN	Input	CR Cb – Blue Chroma Component
CR_CR_IN	Input	CR Cr – Red Chroma Component
CR_IVLD	Input	CR Input Valid (Optional)
<b>Output Interface</b>		
CR_Y_OUT	Output	CR Y' – Luma Component
CR_CB_OUT	Output	CR Cb – Blue Chroma Component
CR_CR_OUT	Output	CR Cr – Red Chroma Component
CR_CBCR_OUT	Output	CR CBCR Muxed Blue Red Chroma Components
CR_OVLD	Output	CR Output Valid (Optional)

**Table 1: DB1820 – I/O Pin Description of Chroma Resampler**

## **Verification Method**

The DB1820 contains a test suite with bus functional models that program the DB1820 control & status registers, drives the DB1820 with 4:4:4 Y'CbCr component video data along with timing control, and checks expected 4:2:2 Y'CbCr results.

## **Customer Evaluation**

Digital Blocks offers a variety of methods for prospective customers to evaluate the DB1820. These include Verilog simulations, encrypted FPGA models, or the DB1820 Demo System, which includes an Altera FPGA and 320x240 TFT LCD panel.

## **Deliverables**

The DB1820 is available in FPGA netlist or synthesizable RTL Verilog, along with Synopsys Design Constrains, a simulation test bench with expected results, reference design, and user manual.

## **Support**

The DB1820 IP Core is warranted against defects. One year of phone and email technical support is included, starting with the first interaction. Additional maintenance and support options are available.

## **Ordering Information**

Please contact Digital Blocks for additional technical, pricing, evaluation, and support information.

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