

General Description

The Digital Blocks DB1840 CCIR 656 Decoder IP Core decodes an ITU-R BT.656 digital video uncompressed NTSC 720x486 (525/60 Video System) and PAL 720x576 (625/50 Video System) Standard Definition frame, extracting Y’CbCr 4:2:2 video components, optional Ancillary Data, and frame timing & status signals.

Figure 1 depicts the DB1840 CCIR 656 Decoder IP Core embedded within an integrated circuit device. Control & Status can be programmed into optional DB1840 registers via a bus interface, or set as non-register fixed parameters at synthesis.

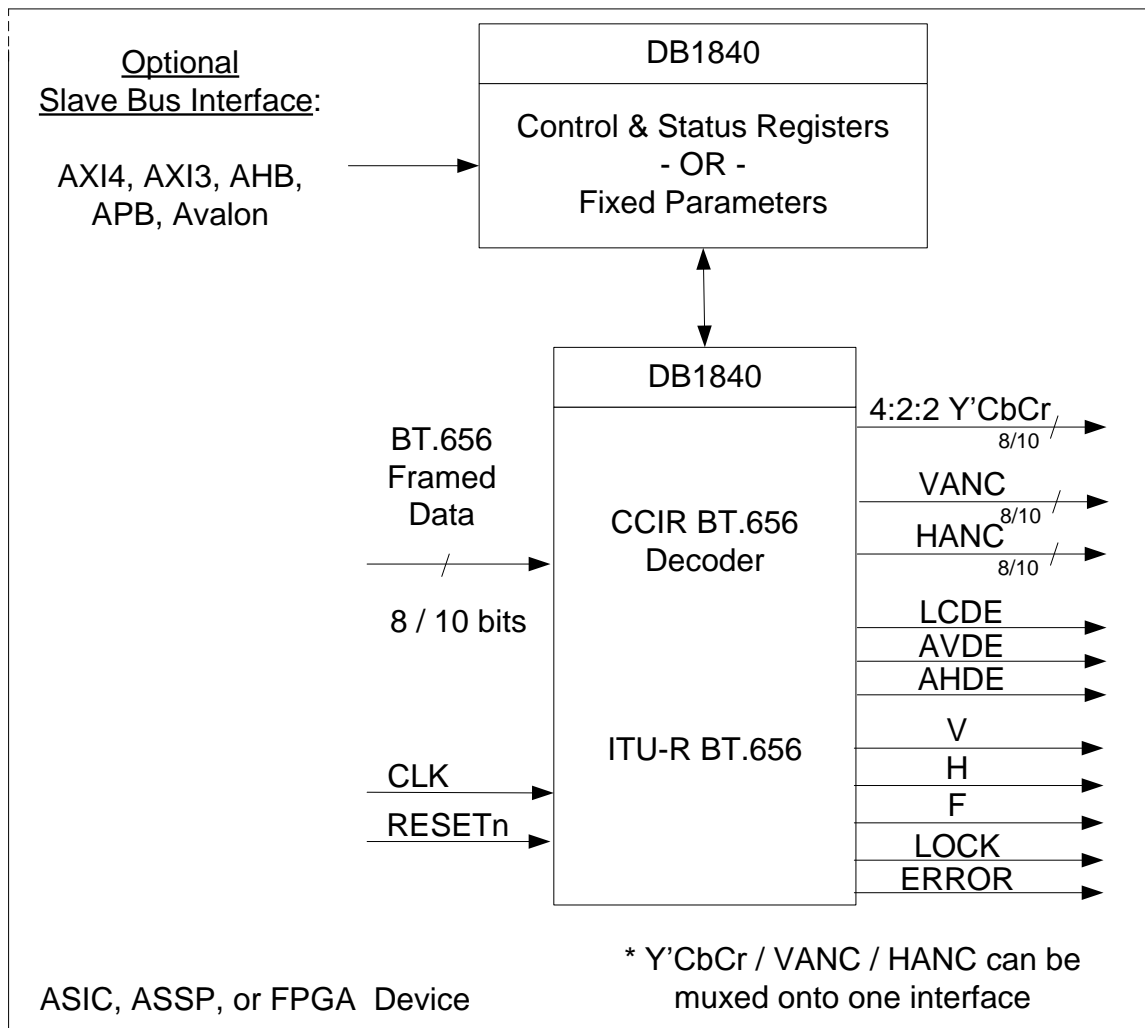


Figure 1: DB1840 CCIR 656 Decoder

Features

- Decodes an CCIR ITU-R BT.601 Frame providing the following outputs:
 - Y'CbCr color digital components (Luma/Chroma)
 - Data Enable for Luma / Chroma component samples
 - V, H, F timing synchronization
 - Status - Lock & Error detection
- Decodes optionally the following:
 - Vertical / Horizontal Ancillary Data
 - Data Enables for Vertical / Horizontal Ancillary Data
- Optional 8/10-bit Data extraction
- Supports following Standard Definition:
 - NTSC 720x486 (525/60 Video System)
 - PAL 720x576 (625/50 Video System)
- 27 MHz Sampling Rate
- User optional Slave Bus Interface for programming Control & Status Registers
- Optional Features:
 - FIFO – for buffering & separate clock domain interface
 - Chroma Re-sample to 4:4:4 Y'CbCr
 - Color Space Conversion from Y'CbCr to RGB
- Member of Digital Blocks' *Video Signal & Image Processing IP Core Family*, which include the following:
 - DB1800 - Standard Definition NTSC/PAL/SECAM Video Sync Separator
 - DB1810 - Color Space Convert
 - DB1820 - Chroma Resampler
 - DB1825 - RGB to YCrCb Color Space Convert with 4:4:4 to 4:2:2 Chroma Resampler
 - DB1830 – CCIR BT.656 Encoder
 - DB1840 – CCIR BT.656 Decoder
 - DB1892 - RGB to CCIR601/656 Encoder
- On-Chip Interconnect Compliance (optional) – Avalon/Qsys, AXI, AXI4, AHB:
 - AMBA AXI4 Protocol Specification (V3.0)
 - AMBA AXI3 Protocol Specification (V1.0)
 - AMBA AHB Specification 2.0
 - AMBA APB Specification 2.0
 - Avalon Interface Specification (MNL-AVABUSREF-2.0)
- FPGA Integration Support:
 - Altera Quartus II & Qsys / SOPC Integration & NIOS II EDS Reference Design

- Xilinx ISE Design Suite utilizing AMBA AXI4 & Embedded Development & Software Development Kits
- ASIC / ASSP Design-In Support:
 - Compliance to RTL Design & Coding Standards
 - Digital Blocks Support Services
- Fully-synchronous, synthesizable Verilog RTL IP Core, with rising-edge clocking, No gated clocks, and No internal tri-states

Pin Description

DB1840 CCIR 656 Decoder contains optional AMBA bus AXI4, AXI3, AHB, APB and Avalon bus for processor programming of internal parameters. The DB1840 optionally contains no bus interface with hard-coding of the video transformation parameters.

The DB1840 contains the following I/O interface. For information on a bus fabric interface I/O, please contact Digital Blocks.

Name	I/O Type	I/O Size	Description
Input Interface			
BT656_CLK	Input	1	BT656 Sample Clock (27 MHz)
BT656_RESETh	Input	1	BT656 Reset
BT656_FRAME_DATA	Input	8/10	BT656 Frame Data
Output Interface			
BT656_YCRCB_DATA	Output	8/10	BT656 Decoder Output (8/10-bits)
BT656_LCDE	Output	1	Data Enable – Luma/Chroma Components
BT656_V	Output	1	BT656 Vertical Sync
BT656_H	Output	1	BT656 Horizontal Sync
BT656_F	Output	1	BT656 Field 1,2
BT656_LOCK	Output	1	BT656 Frame Lock
BT656_ERROR	Output	1	BT656 Parity Error Detected
Optional Interface			
BT656_VANC	Output	8/10	BT656 Decoder Vertical Ancillary Data Output (8/10-bits)
BT656_HANC	Output	8/10	BT656 Decoder Horizontal Ancillary Data Output (8/10-bits)
BT656_AVDE	Output	1	Data Enable – Ancillary Vertical Data
BT656_AHDE	Output	1	Data Enable – Ancillary Horizontal Data

Table 1: DB1840 – I/O Pin Description of CCIR 656 Decoder

Verification Method

The DB1840 contains a test suite with bus functional models that program the DB1840 control & status registers, drives the DB1840 with various standard BT.656 Frames and checks component color data and timing synchronization signal output expected results.

Customer Evaluation

Digital Blocks offers a variety of methods for prospective customers to evaluate the DB1840. These include Verilog simulations and encrypted FPGA model. Please contact Digital Blocks for more information.

Deliverables

The DB1840 is available in FPGA netlist or synthesizable RTL Verilog, along with Synopsys Design Constrains, a simulation test bench with expected results, reference design, and user manual.

Support

The DB1840 IP Core is warranted against defects. One year of phone and email technical support is included, starting with the first interaction. Additional maintenance and support options are available.

Ordering Information

Please contact Digital Blocks for additional technical, pricing, evaluation, and support information.

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