

### General Description

Digital Blocks DB1881AHB IP Core interfaces a Camera CMOS Image Sensor to Frame Buffer Memory via the AMBA AHB Interconnect. The DB1881AHB process either RAW Bayer or CCIR656 YCbCr and bursts the video to AHB memory. From there a Display Controller (such as Digital Blocks DB9000) drives the display panel.

The DB1881AHB is a Verilog IP Core targeting FPGA, ASIC, or ASSP devices. Figure 1 depicts the system view of the DB1881AHB Camera Interface IP Core embedded within an integrated circuit device.

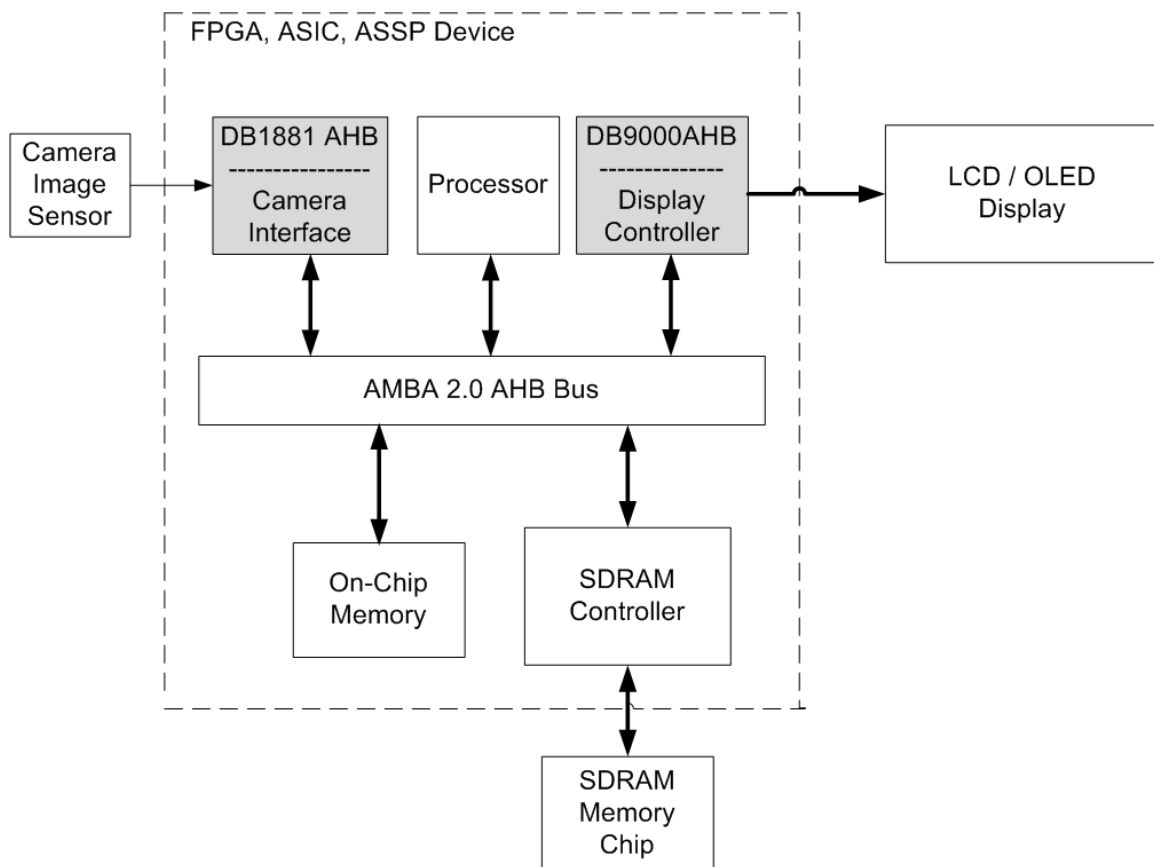


Figure 1: DB1881AHB Camera Interface – System Diagram

### Block Diagram

Figure 2 depicts the DB1881AHB Camera Interface high-level Micro-Architecture (grey items are optional functional blocks). The DB1881AHB accepts RAW Bayer and performs Pixel Defect Detection & Correction and optionally Bayer Demosaicing. Likewise, the DB1881AHB accepts ITU-R BT.656 and performs CCIR656 Frame Decoding and optionally Chroma Up-Converting, and Color Space Conversion.

The RGB video streams into a clock-domain crossing FIFO and is read out by a DMA Controller, sending the video to Frame Buffer Memory connected to the AHB Bus.

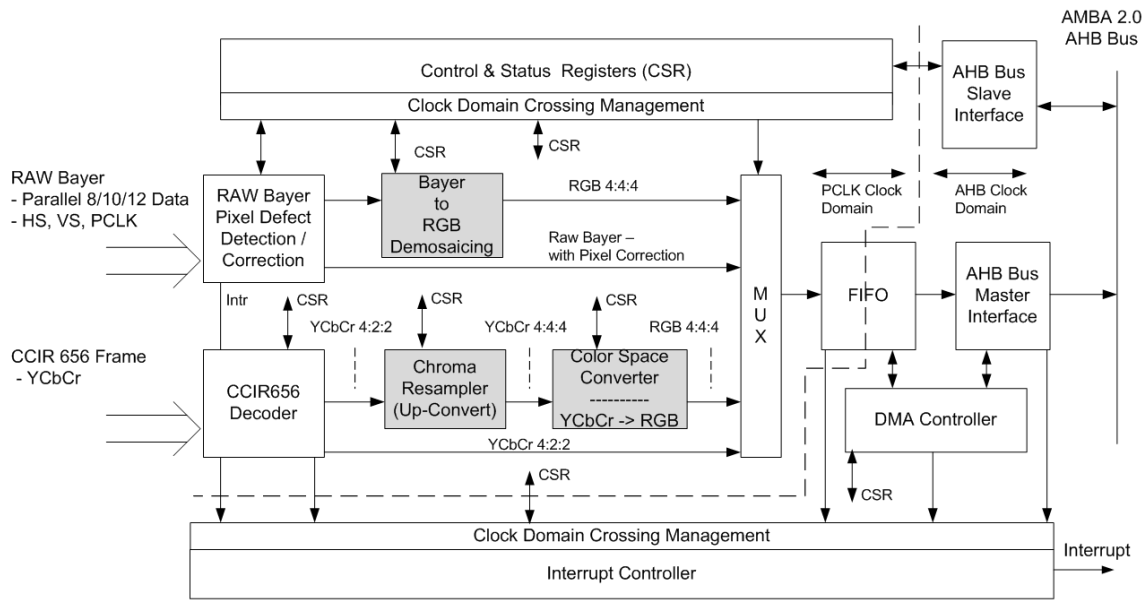


Figure 2: DB1881AHB Camera Interface - Video Signal Processing & DMA to AHB-Based Frame Buffer Memory

## Features

- Camera Interface Options:
  - RAW Bayer:
    - Parallel CMOS 8/10-bit Data
    - Vsync, Hsync, Pixel Clock
  - CCIR656:
    - Serial ITU-R BT.656 Encoded Frame, 8/10-bit Data
    - Clock
  - Resolutions up to 1920x1080p FHD @ 60 fps
- Video Signal Processing (from RAW Bayer or CCIR656):
  - RAW Bayer Pixel Defect Detection & Correction
  - RAW Bayer Demosaicing – bilinear interpolation
  - CCIR656 Frame Decoder - Outputs ITU-R BT.601 4:2:2 YCbCr
    - Chroma Resampler – Up-converts 4:2:2 YCbCr to 4:4:4 YCbCr sampling (optional)
    - Color Space Conversion (optional):
      - Converts 4:4:4 YCbCr to 4:4:4 RGB
      - FIR Filter with Programmable Coefficients
  - Both RAW Bayer Demosaicing and CCIR656 Frame Decoder outputs Vsync to DMAC. For CCIR656 Frame Decoder, delay added to Vsync output to correspond to pixel delay through Chroma Resampler and Color Space Conversion pipelines.
- Output Buffer:
  - Dual-clock FIFO supporting clock-domain crossing
  - configurable in depth and width
- DMA Controller:
  - Four (4) programmable Base Address Registers supporting 1-4 Frame Buffers: Single, Dual Ping-Pong, 1-2-3 and 1-2-3-4 circular
  - Burst data to Frame Buffer via AHB Master Bus
- AHB Master Interface – DMAC bursts video samples under DMAC control to Frame Buffer Memory:
  - 32-bit interface, supporting data writes only (64/128/256-bit data interfaces available)
  - INCR, INCR4, INCR8, and INCR16 word bursts
  - Generates address sequences for unspecified and fixed-length bursts
  - Generates **HBUSREQM** requests and monitors & responds to **HGRANTM** grant and **HREADYM**
  - Asserts interrupt MBE error response during bursts

- AHB Slave Interface – Processor interface to Control/Status Registers:
  - Two cycle address & data phases
  - 32-bit data interface, supporting both reads/writes
  - SINGLE word burst
  - OKAY response only
  - Full AHB or AHB-Lite
- Interrupt Controller:
  - 5 sources of internal interrupts (more to be identified)
  - Interrupt Status, Mask, Vector Registers
- Compliance with following AHB Specifications:
  - AMBA Specification Rev 2.0 (AHB Full Protocol for Master & Slave will be used)
  - AMBA 3 AHB-Lite V1.0 (AHB-Lite Protocol is an option)
- Fully-synchronous, synthesizable Verilog RTL core, with rising-edge clocking, No gated clocks, and No internal tri-states.

## **Deliverables**

The DB1881AHB is available in RTL Verilog-2001, along with synthesis scripts, a simulation test bench with expected results, datasheet, and user manual.

## **Ordering Information**

Please contact Digital Blocks for additional technical, pricing, evaluation, and support information.

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