Semiconductor IP

General Description

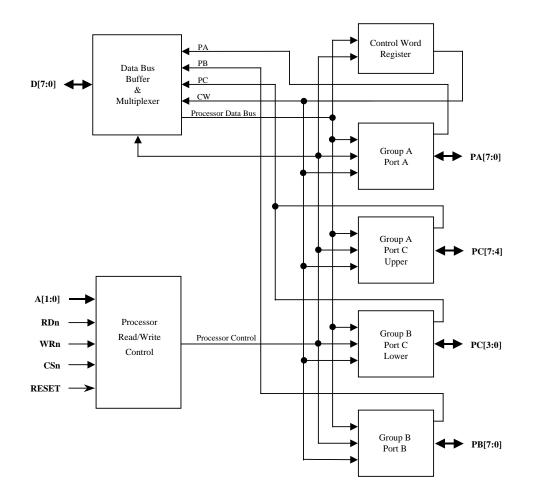
The Digital Blocks DB8255A Programmable Peripheral Interface core is a full function equivalent to the Intel 8255A / 82C55A and Intersil 82C55A devices.

The DB8255A implements a general-purpose I/O interface connecting peripheral equipment to a microprocessor system bus. The core generates 24 programmable I/O lines which are individually programmed in 2 groups of 12 and used in 3 major modes of operation.

Features

The DB8255A contains the following features:

- 24 programmable I/O lines
- 8-bit bidirectional data bus with standard microprocessor interface controls
- Three Modes of operation:
 - Mode 0: Basic Input/Output:
 - 2 groups of 12 I/O lines may be programmed in sets of 4 and 8 to be inputs or outputs.
 - Mode 1: Strobed Input/Output:
 - Each group may be programmed to have 8 lines of input or output. The 3 of the remaining 4 lines are used for handshaking and interrupt control signals.
 - Mode 2: Bidirectional Bus
 - Single 8-bit bidirectional bus for both transmitting and receiving data
- Control Word Read-Back Capability
- Direct Bit Set/Reset Capability
- RESET input clears the Control Register and all 24 programmable I/O lines set to input mode
- Available in VHDL, Verilog, or FPGA-Specific Netlist



Block Diagram

Figure 1: DB8255A Programmable Peripheral Interface Block Diagram

Functional Description

The DB8255A core is partitioned into modules as shown in Figure 1 and described below.

Data Bus Buffer

The 3-state, bi-directional 8-bit buffer is used to interface the DB8255A core to the microprocessor system data bus. Data, control words and status information are transferred through the Data Bus Buffer.

Processor Read / Write Control Logic

The Processor Read / Write Control Logic processes all internal and external transfers of both Data and Control or Status words. It accepts inputs from the microprocessor Address and Control busses and in turn, issues commands to both of the Control Groups.

Group A and Group B Controls

The functional configuration of each port is programmed by systems software. In essence, the microprocessor "outputs" a control word to the DB8255A. The control word contains information such as "mode", "bit set", "bit reset", etc., that initializes the functional configuration of the DB8255A.

Ports A, B, and C

The DB8255A contains three 8-bit ports (A, B, and C). All can be configured in a wide variety of functional characteristics by the system software but each has its own special features to further enhance the flexibility of the DB8255A.

Port A. One 8-bit data output latch/buffer and one 8-bit input latch buffer.

Port B. One 8-bit data input/output latch/buffer.

Port C. One 8-bit data output latch/buffer and one 8-bit data input buffer (no latch for input). This port can be divided into two 4-bit ports under the mode control. Each 4-bit port contains a 4-bit latch and it can be used for the control signal outputs and status signal inputs in conjunction with ports A and B.

Verification Methods

The DB8255A Programmable Peripheral Interface core's function was verified by means of a proprietary hardware modeler. The same stimulus was applied to a hardware model that contained the original Intel 8255A chip, and the results compared with the core's simulation outputs. The DB8255A has been verified in silicon via customer designs.

Pin Description

Name	Туре	Polarity	Description
D[70]	Bidir	-	Data Bus
A[10]	In	-	Address
RDn	In	Low	Read Control
WRn	In	Low	Write Control
CSn	In	Low	Chip Select
RESET	In	High	Reset
PA[70]	Bidir	-	Port A
PB[70]	Bidir	_	Port B
PC[70]	Bidir	-	Port C

Table 1: DB8255A Programmable Peripheral InterfaceI/O Pin Description

Deliverables

The DB8255A Programmable Peripheral Interface is available in synthesizable RTL VHDL source or in an EDIF netlist. The IP Core comes with a comprehensive test suite, synthesis scripts, data sheet, and user manual. The test suite includes a testbench, test vectors and expected results.

Ordering Information

Please contact Digital Blocks for additional technical, pricing, and support information.

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