Digital Blocks

Semiconductor IP

DB8259S

Programmable Interrupt Controller

General Description

The Digital Blocks DB8259S Programmable Interrupt Controller core is a full function equivalent to the Intel 8259A / Intersil 82C59A / NEC uPD8259A devices.

The DB8259S Interrupt Controller manages up to eight vectored priority interrupts for a microprocessor. Using multiple instantiations of the DB8259S core and programming it to cascade mode enables up to sixty-four vectored priority interrupts. More than sixty-four vectored interrupts can be accomplished by programming the DB8259S core to Poll Command Mode. Interrupt sources may be either edge or level triggered.

Features

The DB8259A supports eight vectored priority interrupts per core, sixty-four vectored priority interrupts with cascading, and more than sixty-four vectored interrupts with programming in Poll Command Mode.

- Programming for all 8259A modes and operational features:

    o MCS-80/85 and 8088/8086 processor modes

    o Fully Nested Mode and Special Fully Nested Mode

    o Special Mask Mode & Buffered Mode

    o Poll Command Mode

    o Cascade Mode with Master or Slave selection

    o Automatic End-of-Interrupt Mode

    o Specific and Non-Specific End-of-Interrupt Commands

    o Automatic & Specific Rotation

    o Edge and level triggered interrupt input modes

    o Reading of Interrupt Request Register (IRR) and In-Service Register (ISR) through data bus

    o Writing and reading of Interrupt Mask Register (IMR) through data bus

- Cost-effective CPLD/FPGA replacement solution for 8259A merchant components (Intel/Intersil/NEC). Ideal for ASIC implementations.

- Available in VHDL, Verilog, or FPGA-Specific Netlist
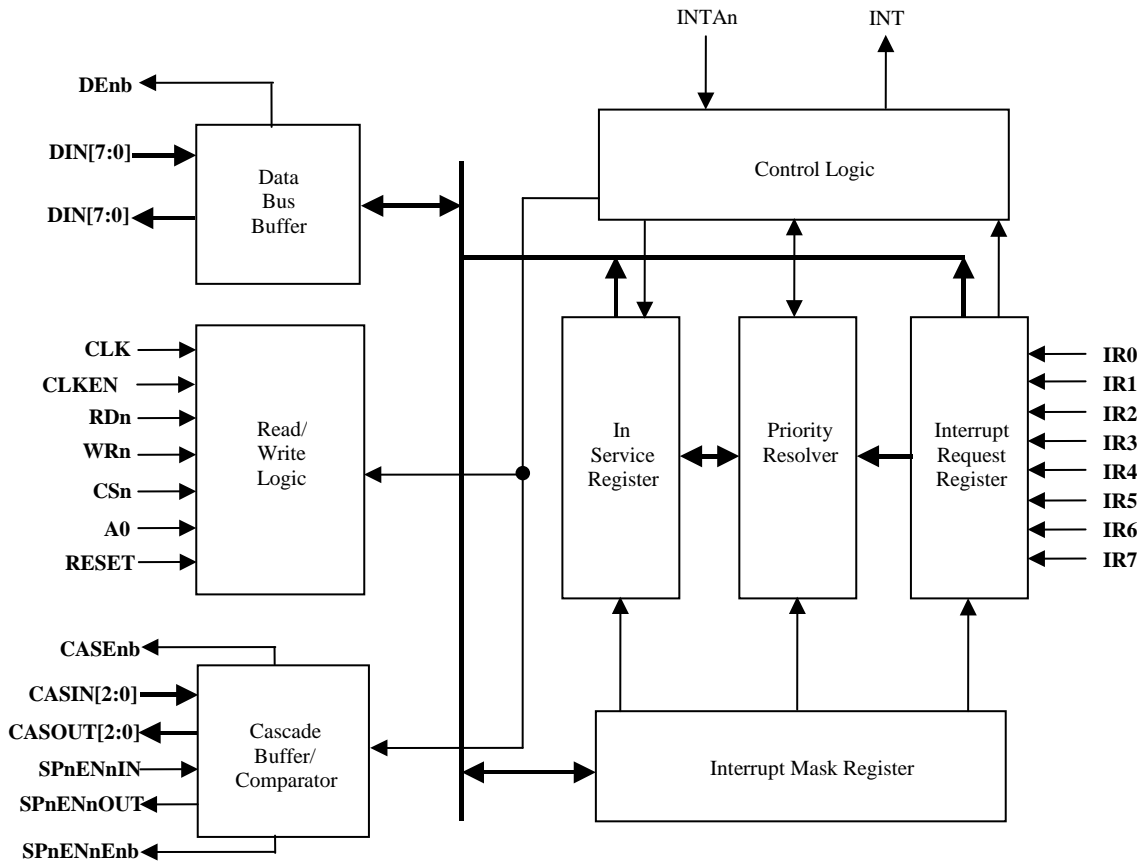
Block Diagram

Figure 1: DB8259S Programmable Interrupt Controller Block Diagram

Functional Description

The DB8259S core is partitioned into modules as shown in Figure 1 and described below.

Data Bus Buffer

The 3-state, bi-directional 8-bit buffer is used to interface the DB8259S core to the microprocessor system data bus. Control words and status information are transferred through the Data Bus Buffer.

Read / Write Logic

The Read / Write Logic processes the data bus control signals and stores the output commands from the microprocessor. The commands are the four Initialization Command Word (ICW) registers and the three Operation Command Word (OCW) registers. These

registers contain the various programming control formats for device operation. The Read/Write Logic block also enables the status of the DB8259S core to be transferred to the system data bus.

The CLK and CLKEN inputs facilitate an all synchronous design. All digital logic is clocked with CLK, enabling integration into FPGA and ASIC synchronous design flows. CLKEN facilitates system data bus connectivity to the microprocessor, and is typically connected to a wait state logic output signal. For 386EX microprocessors, CLKEN can be simply connected to the 386EX CLKOUT signal. For fast system bus applications, CLKEN can be not used by tying to its active (or always enabled) GND level.

Cascade Buffer Comparator

The Cascade Buffer Comparator stores and compares the IDs of all DB8259S cores instantiated in the system. The associated three I/O pins (CAS0-2) are outputs when the DB8259S is used as a Master and are inputs when the DB8259S is used as a Slave. As a Master, the DB8259S core sends the ID of the interrupting slave device onto the CAS0-2 lines. The selected Slave will send its preprogrammed subroutine address onto the system data bus during the next one or two consecutive INTAn pulses.

Control Logic

The Control Logic checks for INTAn pulses which cause the DB8259S to release vector information onto the system data bus. The format of this data depends on the system mode of the DB8259S. This block also sets the interrupt output high whenever a valid interrupt request is asserted.

Interrupt Request Register (IRR) and In-Service Register (ISR)

The interrupts at the IR input lines are handled by two registers in tandem, the Interrupt Request Register (IRR) and the In-Service Register (ISR). The IRR is used to store all the interrupt levels which are requesting service. The ISR is used to store all the interrupt levels that are being serviced by the microprocessor.

Priority Resolver

The Priority Resolver determines the priorities of the bits set in the IRR. The highest priority is selected and strobed into the corresponding bit of the ISR during an INTAn cycle.

Interrupt Mask Register (IMR)

The Interrupt Mask Register (IMR) stores the bits that control the interrupt lines to be masked. The IMR operates on the IRR. Masking of a higher priority input will not affect the interrupt request lines of lower priority.

Verification Methods

The DB8259S Programmable Interrupt Controller cores function was verified by means of a proprietary hardware modeler. The same stimulus was applied to a hardware model that contained the original Intel 8259A chip, and the results compared with the core's simulation outputs. The DB8259S has been verified in silicon via customer designs.

Pin Description

Name	Type	Polarity	Description
reset	In	High	Power-up Reset
clk	In	-	Clock
clken	In	Low	Clock Enable
a0	In	-	Address
rdn	In	Low	Read Control
wrn	In	Low	Write Control
csn	In	Low	Chip Select
ir[7..0]	In	Edge/ High Level	Interrupt Request
din[7..0] [1]	In	-	Data Bus Inputs
casin[2..0] [1]	In	-	Cascade Line Inputs
spnennin [1]	In	-	Slave Program Input Buffer
dout[7:0] [1]	Out	-	Data Bus Outputs
casout[2:0] [1]	Out	-	Cascade Line Outputs
spnennout [1]	Out	-	Buffer Transceiver Enable
denb [1]	Out	High	Data Bus Output Enable
casenb [1]	Out	High	Cascade Line Output Enable
spnennenb [1]	Out	High	Slave Program/Buffer Transceiver Enable Controller
int	Out	High	Interrupt (to processor)

[1] Listed are the unidirectional I/Os for din[7..0], dout[7:0], casin[2..0], casout[2:0], spnennout, and spnennin. The DB8259S comes with a wrapper to map these I/Os to match the bidirectional I/Os of the original 8259A device, resulting in 29 I/O pins.

Table 1: DB8259S Programmable Interrupt Controller I/O Pin Description

Deliverables

The DB8259S Programmable Interrupt Controller is available in synthesizable RTL VHDL or Verilog source or FPGA-specific netlist. The IP Core comes with a comprehensive test suite, synthesis scripts, data sheet, and user manual.

Ordering Information

Please contact Digital Blocks for additional technical, pricing, and support information.

Digital Blocks, Inc.
PO Box 192
587 Rock Rd
Glen Rock, NJ 07452 USA
Phone: +1-201-251-1281
eFax: +1-702-552-1905
info@digitalblocks.com