General Description

The Digital Blocks DB9000AHB5 Display Controller IP Core interfaces a microprocessor and frame buffer memory via the AMBA 5 AHB bus fabric to a TFT LCD or OLED display panel. It is the DB9000AHB-Lite core re-based on the AMBA 5 AHB protocol, for SoCs and FPGA subsystems whose fabric has moved from AMBA 3 AHB-Lite to AMBA 5 AHB.

AMBA 5 AHB is defined as a base protocol plus a set of optional properties, and the DB9000AHB5 follows that model: each property below is an independent synthesis option. With every optional property disabled the master and slave ports present the AHB-Lite signal set, so the DB9000AHB5 drops into an existing AHB-Lite subsystem unchanged.

In an FPGA, ASIC or ASSP device the microprocessor is typically an ARM Cortex-M or Cortex-A class processor, and frame buffer memory is either on-chip SRAM or larger off-chip SRAM or SDRAM. Figure 1 depicts the system view of the DB9000AHB5 IP Core embedded within an integrated circuit device; the DB9000AHB5 Master Port can also connect directly to a multi-port memory controller with an AHB port interface.

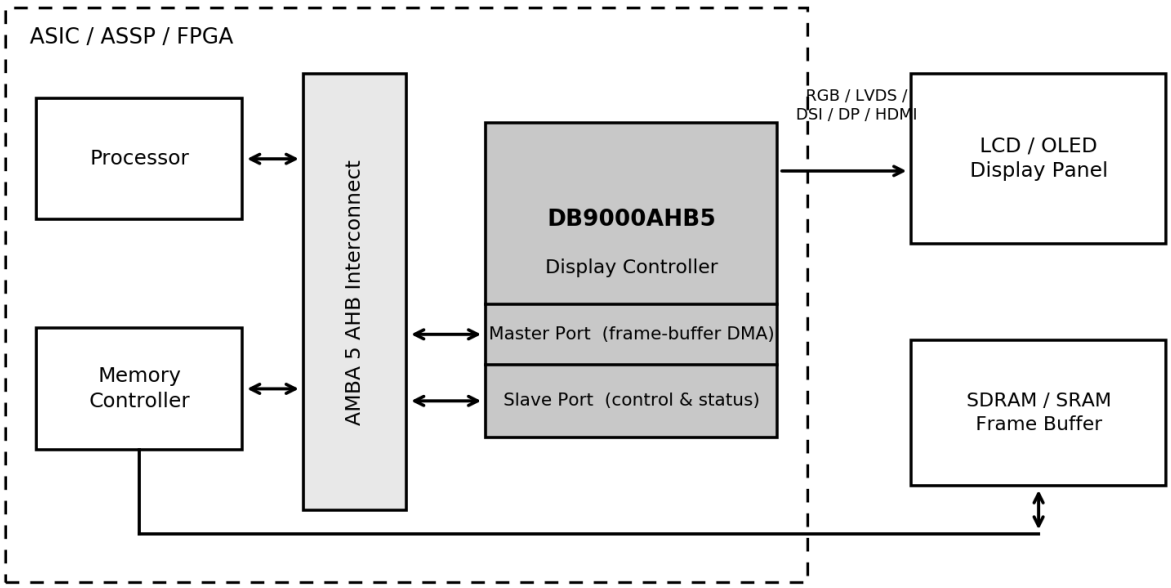

Figure 1: DB9000AHB5 Display Controller System View

AMBA 5 AHB Features

- AMBA 5 AHB Master Port for frame buffer DMA and AMBA 5 AHB Slave Port for control & status, both with the AHB-Lite single-master signalling that suits a point-to-point connection to a multi-port memory controller, and multi-layer AHB interconnect where a shared fabric is used
- Wide data bus support — the AMBA 5 AHB data bus width range extends to 1024 bits, and the DB9000 master data path, Input FIFO width and pixel unpack stage are parameterized to match, so bus width is sized to the panel bandwidth rather than to the protocol
- Extended Memory Types property — the extended HPROT encoding (bufferable, modifiable / cacheable, lookup, allocate, shareable) is driven on frame buffer read bursts, so a cache-coherent AMBA 5 interconnect can classify the display's traffic correctly instead of treating it as legacy non-cacheable
- Secure Transfers property — HNONSEC is driven from a control register field, allowing the frame buffer, overlay windows and cursor buffer to reside in TrustZone-protected memory

- User Signalling property — HAUSER, HWUSER and HRUSER sideband buses of configurable width, for system-specific requester identification and sideband attributes
- Exclusive Transfers property (HEXCL / HEXOKAY) and master identification (HMASTER) on the Slave Port, for register access from a multi-master system
- INCR bursts sized by the Input FIFO fill level, with the AMBA 5 AHB burst-termination rules — no early burst termination is required of the interconnect
- Each property above is an independent synthesis option; all disabled presents the AHB-Lite signal set

Display Controller Features

- Wide range of programmable display panel resolutions:
  - Maximum programmable resolution 4096×4096, from small 320×240 panels upward
  - Horizontal pixel resolutions from 16 to 4096 pixels in 16-pixel increments
- Programmable 1 or 2-port TFT LCD / OLED display panel interface:
  - 18-bit digital (6 bits/color) and 24-bit digital (8 bits/color) parallel RGB
  - Interfaces to LVDS, DVI, HDMI and DisplayPort transmitters
- Programmable frame buffer bits-per-pixel (bpp) color depths:
  - 1, 2, 4, 8 bpp mapped through the Color Palette
  - 16, 18, 24 bpp driving the panel directly (30 bpp with the HDR option)
  - Programmable output format: RGB 6:6:6 / 5:6:5 / 5:5:5 on the 18-bit interface, RGB 8:8:8 on the 24-bit interface
- Color Palette RAM to reduce frame buffer storage and bus bandwidth:
  - 256-entry × 16-bit RAM, implemented as 128 entries × 32 bits
  - Loaded through the Slave Port statically by the microprocessor, or through the Master Port dynamically each frame by the DMA controller
- Programmable horizontal and vertical timing parameters — front porch, back porch, sync width, pixels-per-line, lines-per-panel, and sync polarity
- Programmable pixel clock — divider from 1 to 128 of the bus clock, programmable polarity, or direct drive from an external pixel clock
- Programmable Data Enable timing signal, derived from the horizontal and vertical timing parameters, with programmable polarity
- AMBA 5 AHB interconnect:
  - AMBA 5 AHB Master Port for DMA access of frame buffer memory
  - AMBA 5 AHB (or APB) Slave Port for the control & status interface to the microprocessor
  - Master bus data width configurable to match the memory subsystem
- Three memories:
  - Input FIFO decoupling the bus clock from the panel pixel clock, integrated with the DMA controller
  - 256-word × 16-bit Color Palette RAM
  - Output FIFO
  - FIFOs parameterizable in depth and width
- Power up and down sequencing support, with PWM backlight control
- 9 sources of internal interrupts with masking control
- Little-endian, big-endian, or Windows CE mode
- Compliance with the following specifications:
  - AMBA 5 AHB Protocol Specification
  - AMBA 3 AHB-Lite Protocol Specification v1.0, with all optional AMBA 5 properties disabled
- Fully-synchronous, synthesizable Verilog RTL core, with rising-edge clocking, no gated clocks and no internal tri-states

Display Controller — Block Diagram

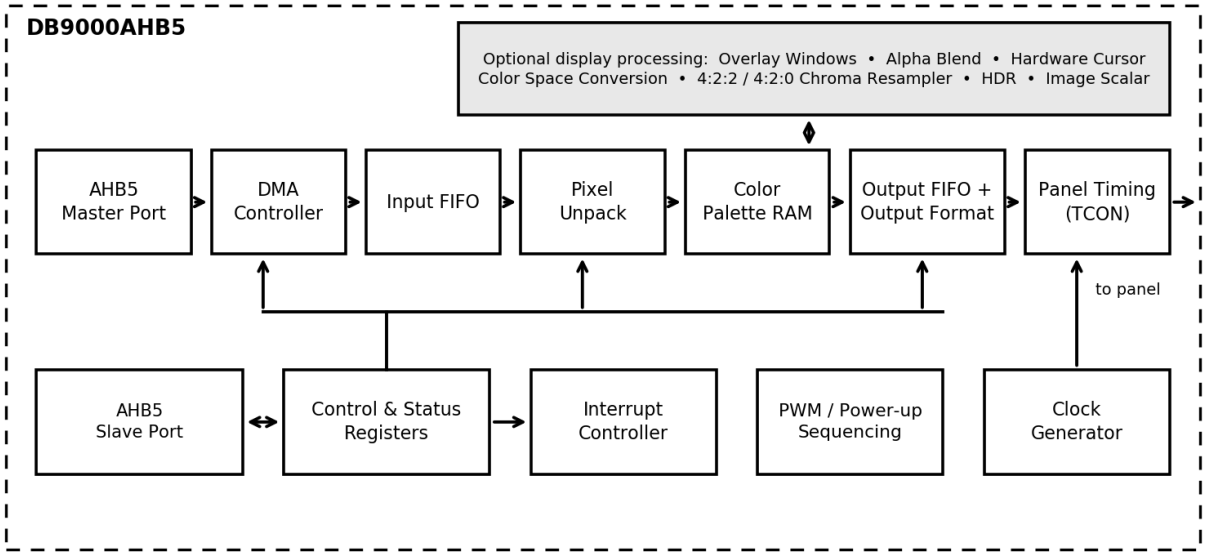

Figure 2: DB9000AHB5 Display Controller Block Diagram

Display Resolution Support — Additional Information

Example high resolutions: 1920×1200, 1920×1080, 1680×1050, 1600×1200, 1600×900, 1440×900, 1366×768, 1280×1024, 1280×768, 1024×768, 1024×600, 1024×576, 960×540, 800×600, 800×480.

Example medium / small resolutions: 640×480, 640×400, 640×240, 640×200, 480×800, 480×640, 480×272, 480×234, 320×240, 320×200, 240×400, 240×320, 240×240.

Configuration Options

Every DB9000 shipment is a synthesizable Verilog RTL core, not a fixed netlist. Bus protocol, bus width, memory technology and FIFO sizing are all set by `define / parameter before synthesis, and each advanced feature is only built into the gate count if it is licensed and enabled — so an unlicensed feature costs zero silicon.

Core Synthesis Parameters — available in every DB9000 configuration, no licensing required.

Parameter	Description
Bus Protocol & Interconnect	AMBA AXI5 / ACE5-Lite, AXI4, AXI3, AHB5, AHB, AHB-Lite, APB, or Altera Avalon-MM — selected by a single Verilog `define.
Master Bus Data Width	32-, 64-, 128-, 256- or 512-bit master bus, sized to the target resolution and bandwidth.
Memory Technology Target	Palette, FIFO and Cursor memories instantiate through one wrapper module, pre-built for Xilinx, Altera, Actel or a generic vendor RAM — or substitute your own.
Synchronous / Asynchronous FIFOs	Input / Output FIFOs default to synchronous; a single `define switches to asynchronous, unregistered-output memories.
Configurable FIFO Depth	Input FIFO address width sets FIFO depth — typically 16 words for small panels, up to 2K words for large, high-resolution panels, with data width scaling to the master bus.
Pixel Clock Source Select	Internal clock-mux architecture with full CR1 programming, or a direct bypass `define that drives the pixel clock straight from PCLK_IN.
Register Bit Trimming	Any unused Control & Status Register bit can be removed and hardwired as a parameter instead — typically halving VLSI footprint versus a fully-populated register set.
DFT Test Bus Passthrough	Optional per-memory DFT test buses netlist up to the top level for scan / BIST insertion.

Licensing & Synthesis Options — optional RTL add-ons, each independently licensable and synthesized only when enabled.

Option	Description

Multi-Window Compositing	
Overlay Windows	1, 2, 4, 8 or 16 independently positioned, DMA-fed overlay windows composited over the base screen, each with its own enable, X/Y start-end and frame-buffer address registers.
Alpha Blend	Per-pixel alpha compositing of an Overlay Window over the base screen at 16 / 18 / 24 bpp, with an 8-bit alpha channel and programmable alpha inversion.
Hardware Cursor	32×32 or 64×64 pixel hardware cursor with its own palette, X/Y positioning and clip registers, sourced from a dedicated dual-port cursor buffer memory — zero host involvement per frame.
Image Scalar (Preliminary)	In-line image scalar within the display controller for ASICs — scaling is applied directly to the pixel stream before it reaches the display interface, with independent scaling per plane.
Color Space & Chroma Processing	
Chroma Resampler — 4:2:2 / 4:2:0	Up-samples packed YCbCr 4:2:2 (2-tap FIR) or planar 4:2:0 video (parallel-DMA, cubic-convolution engine) to 4:4:4 ahead of color-space conversion.
Color Space Conversion	Programmable 4×4 matrix (10-bit signed coefficients, 8-bit summands) converts YCbCr to gamma-corrected RGB, with selectable truncate / round and saturate / clamp behavior; up to three instances — base screen plus two overlay windows.
High Dynamic Range (HDR) (Preliminary)	HDR10 / HLG pixel path: 30 bpp (10:10:10) frame buffers, 10-bit output dithered to 8-bit panels, programmable PQ / HLG / BT.1886 LUTs, a BT.709 ↔ DCI-P3 ↔ BT.2020 gamut matrix in linear light, and BT.2390 tone mapping. ST 2086 metadata sideband. Optional 3D LUT and per-plane HDR.
Advanced Panel Interfaces	
LVDS Serializer (OpenLDI)	OpenLDI V0.95-compliant serializer driven by a customer-supplied 7× pixel clock, generating 18- or 24-bit RGB LVDS output pairs plus VSYNC / HSYNC / DE — Unbalanced mode standard, Balanced mode by request.
Multi-Port / Multi-Link Interface + UHD Output Formatter	1, 2, 4 or 8-lane output to DisplayPort, HDMI, V-by-One, MIPI or LVDS panels, with single / dual / quadrant screen-area partitioning for UHD / 8K displays. Supersedes the earlier fixed 2-port interface as of Release 1.15.0.
Dual Display Support	Splits one unified frame buffer line in half in hardware to drive independent left / right displays from a single pixel pipeline running at 2× pixel clock.
Dynamic Content Engine	
Frame Descriptor Engine	Linked-list DMA engine that reprograms the base-screen and up to 16 overlay-window frame-buffer addresses before every frame with zero host CPU intervention — built for streaming video playout.
Diagnostics & Reliability	
Test Pattern Generation (Preliminary)	On-demand RGB color bars, grayscale gradient or border-grid test patterns triggered by a register write — no external stimulus required.
CRC Check Per Region (Preliminary)	Hardware CRC-802.3 checking of incoming frame-buffer pixel data across 32-, 64-, 128-, 256- or 512-bit bus widths, with programmable per-region checking and automatic retransmission or interrupt on error.
Frozen Display Monitor (Preliminary)	Watchdog-timed monitor of VSYNC / HSYNC / DE and the DMA base-to-current-address heartbeat, with optional automatic self-reset and re-run on a detected fault.

Items marked Preliminary are specified but not yet released; contact Digital Blocks for status. Full register-level detail for every option is documented in the DB9000 Technical Reference Manual.

Options that require sustained high frame-buffer bandwidth — UHD multi-port output, 4:2:0 chroma resampling, HDR — are normally deployed on the AXI variants of the DB9000. Contact Digital Blocks to confirm the configuration for a given panel resolution and bus width.

Pin Description

In addition to the AMBA 5 AHB Master and Slave Bus interfaces, which include the input HCLK and HRESETn signals and the output INTR (interrupt) signal, the interface to the display panel is listed in Table 1. The optional AMBA 5 AHB property signals — extended HPROT, HNONSEC, HAUSER / HWUSER / HRUSER, HEXCL / HEXOKAY, HMASTER — are present only when the corresponding synthesis option is enabled. Note that if the panel is 18-bit data, the lower 6 bits of LCD_R, LCD_G and LCD_B should be connected. In multi-port and multi-link configurations the panel interface is replicated per port.

Name	Type	Description
LCD / OLED Panel Interface		
LCD_PCLK	Output	Pixel Clock
LCD_HSYNC	Output	Horizontal Sync Pulse

LCD_VSYNC	Output	Vertical Sync Pulse
LCD_DE	Output	Display Enable
LCD_PE	Output	Power Enable
LCD_R[7:0]	Output	Red Data
LCD_G[7:0]	Output	Green Data
LCD_B[7:0]	Output	Blue Data

Table 1: DB9000AHB5 — I/O Pin Description for Interface to the Display Panel

Verification Method

The DB9000AHB5 contains a test suite with AMBA 5 AHB bus functional models that program the control & status registers, generate frame buffer data in response to Master read requests, and check expected results, including the optional property signalling where enabled.

The underlying DB9000 display pipeline is silicon-proven and FPGA-proven driving a variety of TFT LCD panels, including NEC and Sharp 320×240, 480×272, 640×480, 800×600 and 1280×768 resolution panels with an 18-bit or 24-bit digital interface.

Customer Evaluation

Digital Blocks offers a variety of methods for prospective customers to evaluate the DB9000AHB5. Please contact Digital Blocks for additional information.

Deliverables

The DB9000AHB5 is available in synthesizable RTL Verilog or technology-specific netlists for FPGAs, along with synthesis scripts, Synopsys Design Constraints (SDC), a simulation test bench with expected results, datasheet, and user manual.

Ordering Information

Please contact Digital Blocks for additional technical, pricing, evaluation, and support information.

Digital Blocks, Inc.
PO Box 192
587 Rock Rd
Glen Rock, NJ 07452 USA
Phone: +1-551-258-0412
info@digitalblocks.com