General Description

The Digital Blocks DB9000AVLN TFT LCD Controller IP Core interfaces a microprocessor and frame buffer memory via the Avalon Bus within Altera Qsys Integration (generating the System Interconnect Fabric) to a TFT LCD panel. In an Altera FPGA, typically, the microprocessor is a NIOS II or ARM processor and frame buffer memory is either on-chip SRAM memory or larger off-chip SRAM or SDRAM. Figure 1 depicts the system view of the DB9000AVLN TFT LCD Controller IP Core embedded within a FPGA.

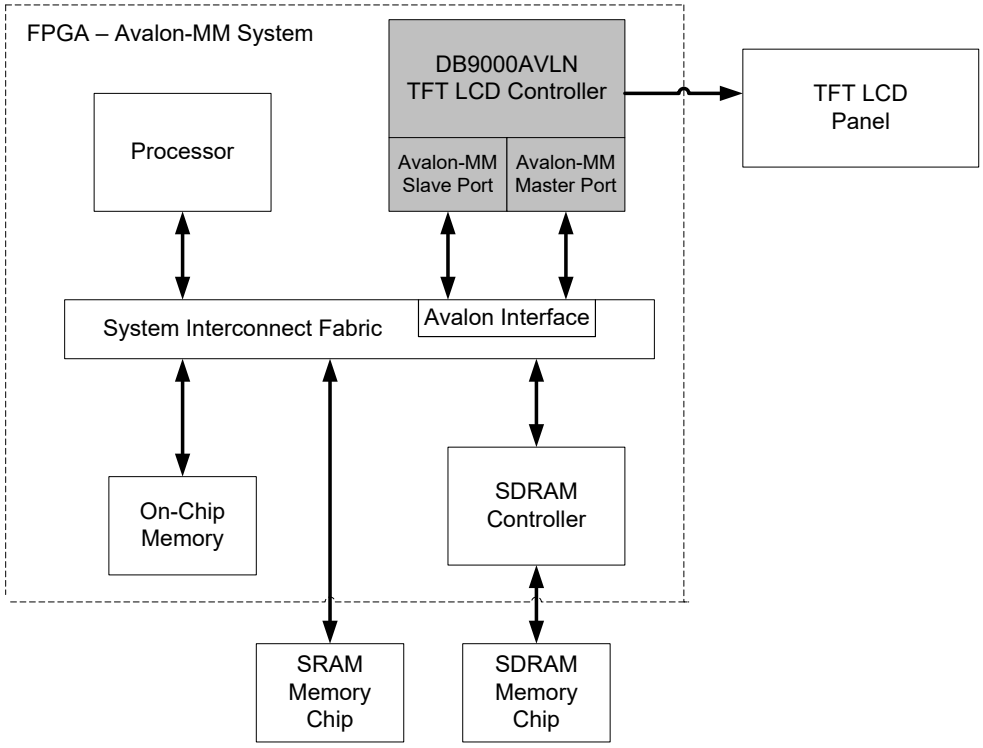

Figure 1: DB9000AVLN TFT LCD Controller – System Diagram

Digital Blocks offers the DB9000 TFT LCD Controller for Altera FPGAs with the Avalon Interface, typically for small- to medium- resolution LCD panels, offering lower logic and power consumption advantages. Digital Blocks offers the DB9000 with AMBA AXI3 / AXI4 Interface typically for medium- to high-resolution LCD panels where higher bus bandwidth access to Frame Buffer memory is required.

Features

- Wide range of programmable LCD Panel resolutions:
  - Maximum programmable resolutions of 4096x4096
  - Horizontal pixel resolutions from 16 to 4096 pixels in 16 pixel increments.
- Example LCD Panel resolutions:
  - 240x240, 240x320, 320x200, 320x240, 480x272
  - 640x200, 640x240, 640x400, 640x480
  - 800x600, 1024x768, 1280x1024
- Programmable 1 Port & 2 Port TFT LCD Panel interfaces
- Interface for 1 Port TFT LCD Panel:
  - 18-bit digital (6-bits/color) LVDS / CMOS
  - 24-bit digital (8-bits/color) LVDS / CMOS
- Interface for 2 Port TFT LCD Panel:
  - Two 24-bit digital (8-bits/color) LVDS / CMOS Ports
- DB9000 interfaces to LVDS, DVI, HDMI, & DisplayPort Transmitters / Receivers
- Programmable frame buffer bits-per-pixel (bpp) color depths:
  - 1, 2, 4, 8 bpp mapped through Color Palette to 18-bit LCD pixel
  - 16, 18, bpp directly drive 18-bit LCD pixel
  - 24 bpp directly drive 24-bit LCD pixel
- Color Palette RAM to reduce Frame Buffer memory storage requirements and Avalon Bus bandwidth:
  - 256 entry by 16-bit RAM, implemented as 128 entry by 32-bits
  - Loaded via the Slave Bus Interface statically by the microprocessor or the Master Bus Interface dynamically with each frame by the DMA controller
- Programmable Output format support:
  - RGB 6:6:6 or 5:6:5 or 5:5:5 on 18-bit digital interface
  - RGB 8:8:8 on 24-bit digital interface
- Programmable horizontal timing parameters:
  - horizontal front porch, back porch, sync width, pixels-per-line
  - horizontal sync polarity
- Programmable vertical timing parameters:
  - vertical front porch, back porch, sync width, lines-per-panel
  - vertical sync polarity
- Programmable pixel clock:
  - pixel clock divider from 1 to 128 of Bus Clock
  - pixel clock polarity
- Programmable Data Enable timing signal:
  - Derived from horizontal and vertical timing parameters

  - display enable polarity
- Three memories:
  - 16-word x 32 bit input FIFO, decoupling Avalon bus & LCD panel clock rates. Integrated with DMA controller.
  - 256-word x 16-bit Color Palette RAM
  - 16-word output FIFO
  - FIFOs parameterizable in depth and width
- Optional Features: Overlay Windows, Color Space Conversion, Alpha Blending, Hardware Cursor
- Power up and down sequencing support
- 9 sources of internal interrupts with masking control
- Little-endian, big-endian, or Windows CE mode
- Compliance with Avalon Interface Specification
- Fully-synchronous, synthesizable Verilog or VHDL RTL core, with rising-edge clocking, No gated clocks, and No internal tri-states

Block Diagram

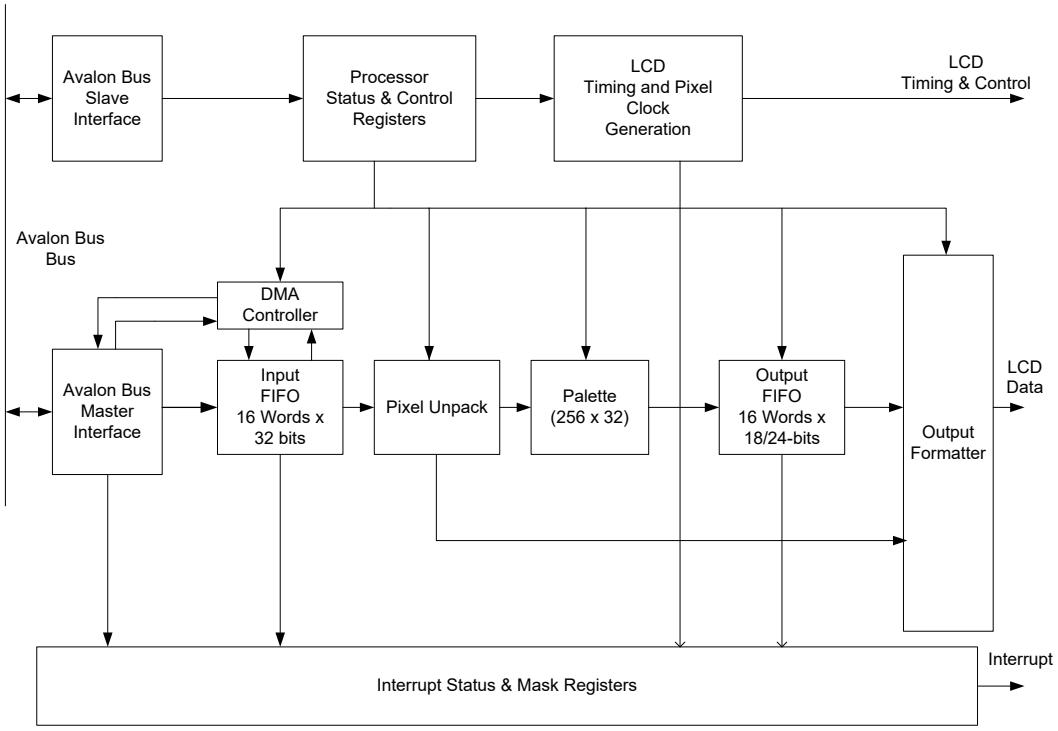

Figure 2: DB9000AVLN Avalon Bus TFT LCD Controller

Pin Description

In addition to the Avalon Master and Slave Bus interfaces, which include the input CLOCK and RESET signals and the output INTR (interrupt) signal, the interface to the

LCD panel is listed in Table 1. Note that if the panel is 18-bits data, the lower 6-bits of LCD_R, LCD_G, and LCD_B should be connected.

Name	Type	Description
LCD Panel Interface		
LCD_PCLK	Output	Pixel Clock
LCD_HSYNC	Output	Horizontal Sync Pulse
LCD_VSYNC	Output	Vertical Sync Pulse
LCD_DE	Output	Display Enable
LCD_PE	Output	Power Enable
LCD_R[7:0]	Output	Red Data
LCD_G[7:0]	Output	Green Data
LCD_B[7:0]	Output	Blue Data

Table 1: DB9000AVLN – I/O Pin Description for Interface to LCD Panel

Implementation Results

The DB9000AVLN IP Core has been implemented in a variety of Altera FPGA devices. Table 2 list example FPGA implementation results using Altera Quartus II Version 17.0. Note the Cyclone IV and V devices are sized for higher resolution panels, requiring higher Memory Bits.

Altera Device	Utilization			Memory Bits	BLK Memory	I/O	Fmax (MHz)
	LEs	ALUTS	ALMs				
Cyclone III EP2C8-C6	1,347	-		4992	4 M4Ks	29	112
Cyclone IV E Speed – C6	1,897			41,344		29	
Cyclone V E / GX / SE Speed - C8			860	41,344		29	120
Stratix III EP2S15-C3	-	1023		4992	4 M4Ks	29	153

Table 2: DB9000AVLN – Altera FPGA Utilization & Performance

Verification Method

The DB9000AVLN contains a test suite with Avalon Bus functional models that program the DB9000AVLN control & status registers, generates frame buffer data in response Avalon Master requests, and checks expected results.

The DB9000AVLN has been verified in separate Altera FPGAs instantiated with the NIOS II and ARM Hard Processor System (HPS) processors, driving a variety of TFT LCD panels, including NEC & Sharp 320x240, 480x272, 640x480, 800x600, and 1280x768 resolution panels with an 18-bit or 24-bit digital interface.

Customer Evaluation

Digital Blocks offers a variety of methods for prospective customers to evaluate the DB9000AVLN. These include Verilog or VHDL simulations, Altera OpenCore models, or the DB9000AVLN Demo System, which includes an Altera FPGA and 640x480 TFT LCD panel. Additional TFT LCD Panel resolutions are available.

Deliverables

The DB9000AVLN is available in Altera netlist or synthesizable RTL Verilog, along with synthesis scripts, a simulation test bench with expected results, reference design, datasheet, and user manual.

Support

The DB9000AVLN IP Core is warranted against defects. One year of phone and email technical support is included, starting with the first interaction. Additional maintenance and support options are available.

Ordering Information

Please contact Digital Blocks for additional technical, pricing, evaluation, and support information.

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