General Description

The Digital Blocks DB9000AXI4-UHD LCD Controller IP Core interfaces a video image in frame buffer memory via the AMBA 3.0 / 4.0 AXI Protocol Interconnect to an 4K/8K TFT LCD / OLED display panel.

The video image in frame buffer memory can be 8/10/12-bit 4:2:0 or 4:2:2 or 4:4:4 sampled YCrCb video or 4:4:4 RGB. For 4:2:0 and 4:2:2 YCrCb, the chroma components are re-sampled to 4:4:4 and color converted to RGB.

Based on Digital Blocks' DB9000AXI4 expertise with 1920 x 1080p Full HD LCD panels, the DB9000AXI4-UHD scales to manage multi-quadrant high definition LCD panels.

The DB9000AXI4-UHD IP Core can be implemented in an ASIC, ASSP, or FPGA device with an embedded microprocessor, an AMBA AXI Interconnect fabric, and SDRAM Controller for access to frame buffer memory. Typically, the microprocessor is an ARC, ARM, Intel, MicroBlaze, MIPS, RISC-V, NIOS II, OpenSPARC, PowerPC, or Tensilica processor and frame buffer memory is off-chip DDR3 / DDR4 SDRAM.

Figure 1 depicts the system view of the DB9000AXI4-UHD LCD Controller IP Core embedded within an integrated circuit device.

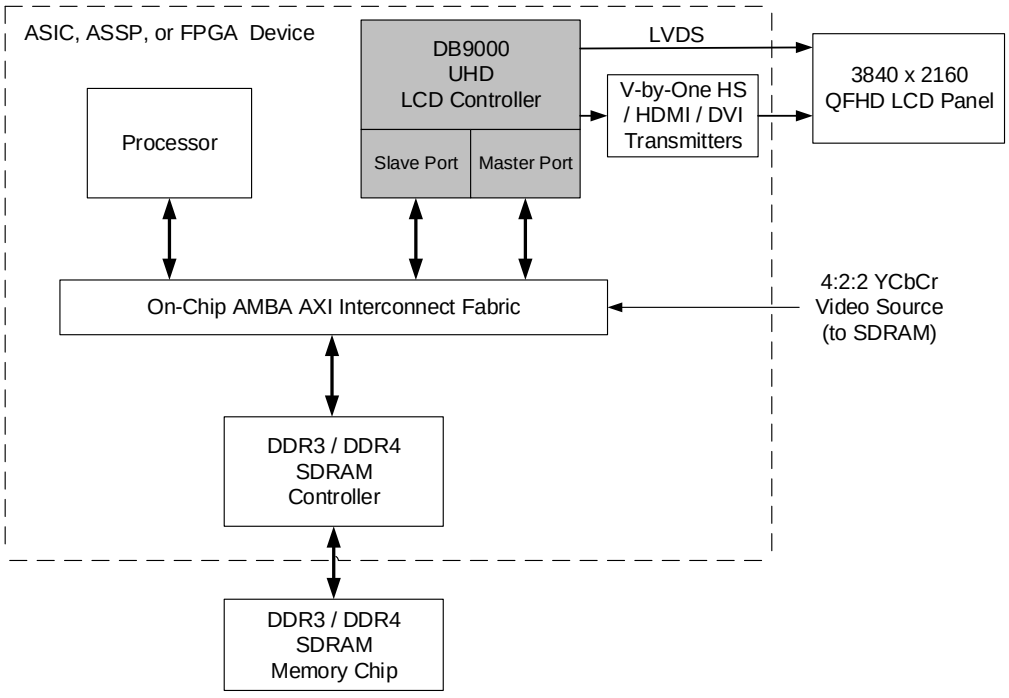

Figure 1: DB9000 UHD LCD Display Controller – System Diagram

Features

- 3840 x 2160 and 7680 × 4320 TFT LCD / OLED Display Panel support
- Additional High Resolution support:
    - Digital Cinema Systems (DCI) 4096 x 2160, 2048 x 1080 2K image, & Cinema Scope HD 2560 x 1080
    - 4096x2560, 3840x2160, 2560x2048, 2048x2048, 2048x1536, 1920x1200, 1920x1080, 1680x1050, 1600x1200
    - 1600x900, 1440x900, 1366x768, 1280x1024, 1280×768, 1080x1920, 1024x768, 1024x600, 1024x576, 960x540, 800x600, 800x480
- High-Resolution TFT LCD Panel support features by AXI Protocol:
    - Up to 16 overlap outstanding reads requests to the SDRAM Controller
    - Quality of Service (QoS) Support (AXI4)
    - Programmable burst lengths up to 16 beats (AXI3) & 256 beats (AXI4)
    - Wide AXI Master Port data width, up to 256-bits
- Optional Features:
    - Video / Graphics Base Screen with up to 16 Overlay Windows
    - αRGB Alpha Blending
    - Color Space Conversion with Chroma Resampler
- Interface for 1,2, 8 Port TFT LCD Panel:
    - 24-bit digital (8 bits/color) LVDS / CMOS
- Interface to LVDS, DVI, HDMI, & DisplayPort Transmitters / Receivers
- Programmable frame buffer bits-per-pixel (bpp) color depths:
    - 8, 10, 12 bits 4:2:2 / 4:4:4 sampled YCrCb
    - 16, 18, 24 bits RGB
- Color Palette RAM to reduce Frame Buffer memory storage requirements and AXI Bus bandwidth (for lower color applications):
    - 256 entry by 16-bit RAM, implemented as 128 entry by 32-bits
    - Loaded via the Slave Bus Interface statically by the microprocessor or the Master Bus Interface dynamically with each frame by the DMA controller
- Programmable horizontal timing parameters:
    - horizontal front porch, back porch, sync width, pixels-per-line
    - horizontal sync polarity
- Programmable vertical timing parameters:
    - vertical front porch, back porch, sync width, lines-per-panel
    - vertical sync polarity
- Programmable pixel clock:
    - pixel clock divider from 1 to 128 of Bus Clock
    - pixel clock polarity
- Programmable Data Enable timing signal:

  - Derived from horizontal and vertical timing parameters
  - display enable polarity
- AMBA AXI4 / AXI3 Interconnect:
  - Selectable 256 / 128 / 64 AXI Master Port for DB9000AXI4 DMA access of frame buffer memory for driving the display
  - Selectable 256 / 128 / 64 AXI or AXI4-Lite Slave Port for control & status interface to microprocessor
- Three memories:
  - N-word x 256 / 128 / 64 bit input FIFO, decoupling AXI bus & LCD panel clock rates. Integrated with DMA controller
  - 256-word x 24-bit Color Palette RAM
  - 16-word output FIFO
  - FIFOs parameterizable in depth and width
- Power up and down sequencing support
- 9 sources of internal interrupts with masking control
- Little-endian, big-endian, or Windows CE mode
- AXI4 Bus - Designed to AMBA AXI Protocol Specification (V2.0)
- AXI3 Bus - Designed to AMBA AXI Protocol Specification (V1.0)
- Support in following Integrated Circuits:
  - ASIC / ASSP with AXI fabric
  - Altera or Xilinx FPGA with AXI fabric
- Fully-synchronous, synthesizable Verilog RTL core, with rising-edge clocking, No gated clocks, and No internal tri-states.

Block Diagram

Figure 2 depicts the DB9000AXI4-UHD LCD Controller IP Core. The controller, with a Video Acquisition Engine, a Base Screen plane + up to 16 Overlay Window video/graphics pixel processor pipelines, and the Ultra HD Output Formatter, builds on Digital Blocks DB9000 family of TFT LCD Controller IP as well as Video Signal Processing IP library.

Note the baseline release of the DB9000AXI4-UHD LCD Controller IP Core supports RGB with the YCbCr support (Chroma Re-sampler & Color Space Converter) an insertion option, depending on customer system requirements.

Likewise, the alpha blend unit is an insertion option, depending on customer composition requirements.

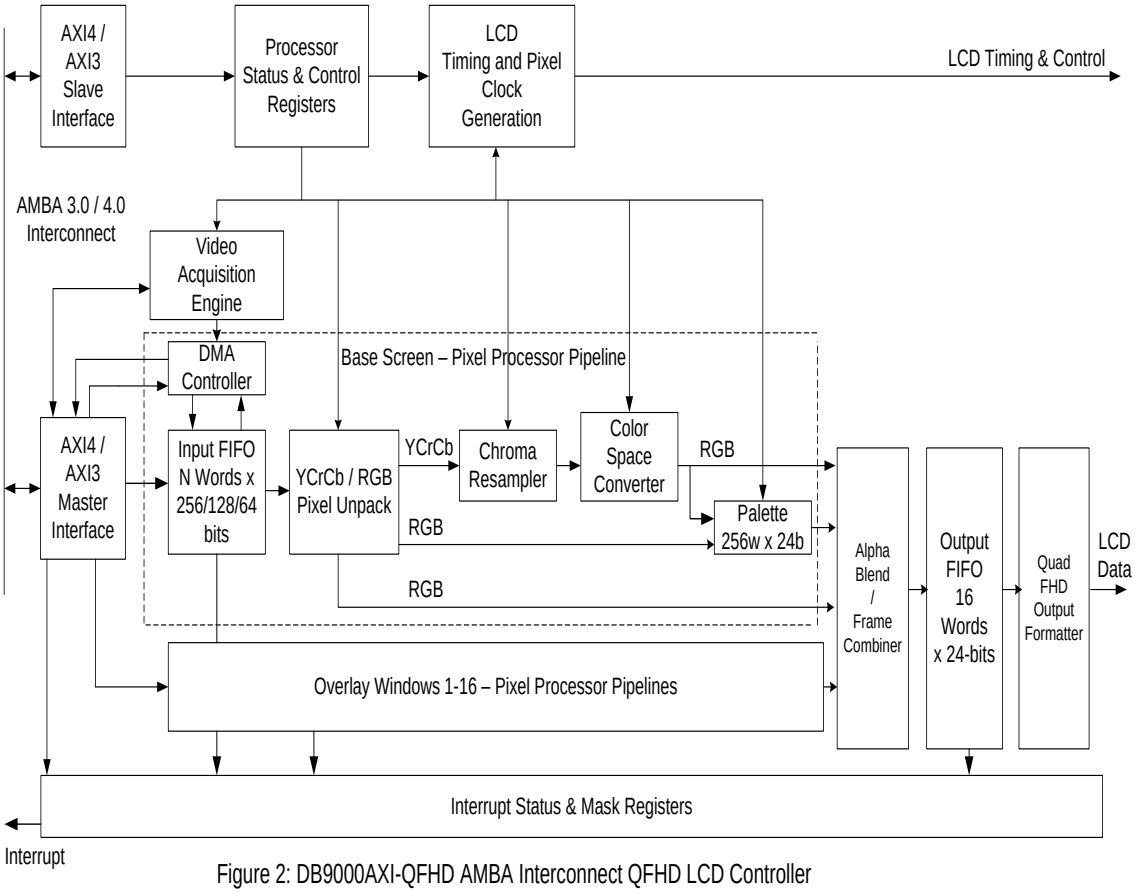

Figure 2: DB9000AXI-QFHD AMBA Interconnect QFHD LCD Controller

Verification Method

The DB9000AXI4-UHD contains a simulation test suite with AXI4 / AXI3 Bus functional models that program the DB9000 control & status registers via the AXI Slave Bus, generates frame buffer data in response to AXI Master requests, and checks expected results.

Customer Evaluation

Digital Blocks offers a variety of methods for prospective customers to evaluate the DB9000AXI4-UHD. Please contact Digital Blocks for additional information.

Deliverables

The DB9000AXI4-UHD is available in synthesizable RTL Verilog, along with a simulation test bench with expected results, datasheet, and user manual.

Ordering Information

Please contact Digital Blocks for additional technical, pricing, evaluation, and support information.

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