General Description

The Digital Blocks DB9000AXI4 Display Controller IP Core interfaces a microprocessor and frame buffer memory via the AMBA AXI4 Protocol Interconnect to a LCD or OLED display panel.

The Display Controller Verilog RTL IP Core comes in a range of releases with advanced display processing, such as Multi-layer Overlay Windows with composition features such as Alpha Blending, Color Space Conversion, 4:2:0 and 4:2:2 YCrCb color with Re-sampling & conversion to RGB, Frame Buffer Compression and Hardware Cursor.

Figure 1 depicts the system view of the DB9000AXI Display Controller IP Core embedded within an ASIC, ASSP, or FPGA device.

System View - Block Diagram

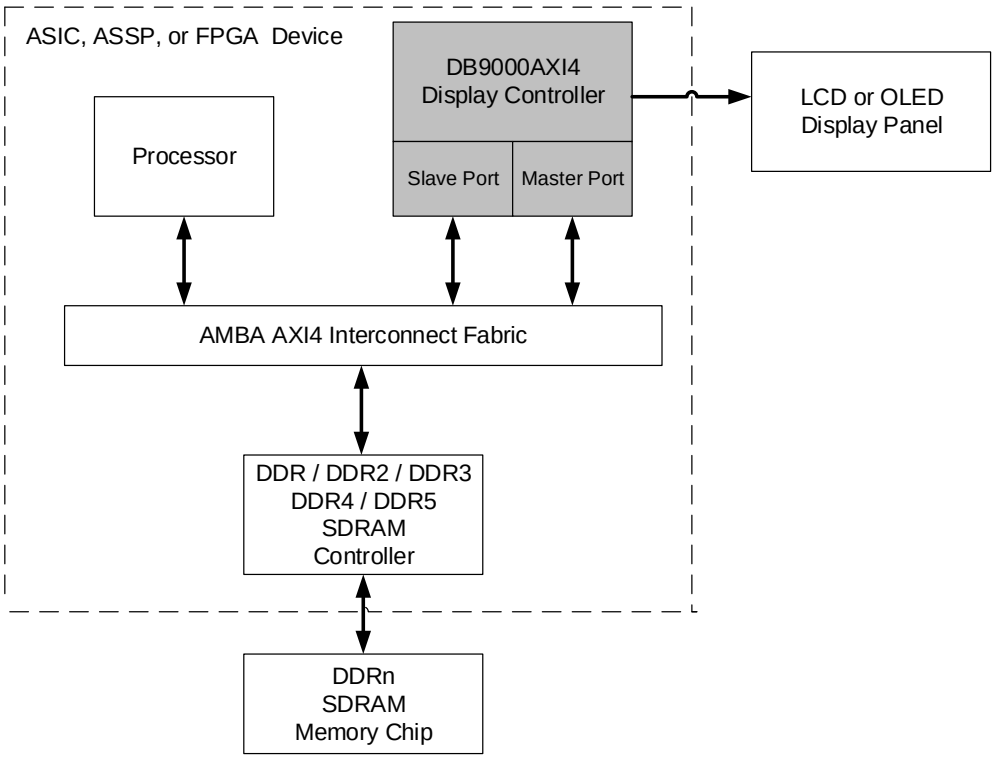

Figure 1: DB9000AXI4 TFT LCD Controller – System Diagram

Features

- Wide range of programmable Display Panel resolutions:
  - Releases for up to 1920x1080 HD, 4K, and 8K
- High-Resolution Display Panel support features by AXI4 Protocol:
  - Up to 16 overlap outstanding reads requests to the SDRAM Controller
  - Quality of Service (QoS) Support
  - Programmable burst lengths up to 256 beats
  - Wide AXI4 Master Port data width, up to 256-bits
- Releases supporting baseline display requirements and releases with following optional display processing features:
  - Overlay Windows with additional options:
    - Alpha Blending
    - Color Space Conversion (CSC)
    - 4:2:0 and 4:2:2 YCrCb with Re-sampling & CSC to RGB
    - Programmable size, placement, & format
  - Hardware Cursor
  - Frame Buffer Compression
  - Many other optional features – contact Digital Blocks with requirements
- Color Palette RAM per layer or single Palette for integrated display image
- Interface to parallel RGB, LVDS, HDMI, DisplayPort, MIPI, Vby1, BT.656
- Programmable 1,2,4,8 Port Display Panel interfaces
- Programmable horizontal & vertical timing parameters:
  - front porch, back porch, sync width, pixels-per-line, lines-per-panel
  - horizontal & vertical sync polarity
- Programmable frame buffer bits-per-pixel (bpp) color depths:
  - 1, 2, 4, 8 bpp mapped through Color Palette
  - 16, 18, 24 bpp non- Palette
- AMBA AXI4 / AHB / APB Interconnect:
  - Selectable 256 / 128 / 64 / 32-bit AXI4 Master Port for DB9000AXI4 DMA access of frame buffer memory for driving the display
  - Selectable 256 / 128 / 64 / 32-bit AXI-lite (or AHB / APB) Slave Port for control & status interface to microprocessor
- Power up and down sequencing support
- 15 sources of internal interrupts with masking control
- Little-endian, big-endian, or Windows CE mode
- Linux OS driver
- Fully-synchronous, synthesizable Verilog RTL core, with rising-edge clocking, No gated clocks, and No internal tri-states.

Display Resolution Support - Additional Information

- Example LCD Panel high resolutions:
  - Digital Cinema Systems (DCI) 2048 x 1080 2K image, 4096 x 2160 4K image, & Cinema Scope HD 2560 x 1080
  - 7680x4320, 4096x2560, 3840x2160, 2560x2048, 2048x2048, 2048x1536, 1920x1200, 1920x1080, 1680x1050, 1600x1200
  - 1600x900, 1440x900, 1366x768, 1280x1024, 1280×768, 1080x1920, 1024x768, 1024x600, 1024x576, 960x540, 800x600, 800x480
- Example LCD Panel medium / small resolutions:
  - 640x480, 640x400, 640x240, 640x200, 480x800, 480x640, 480x272
  - 480x234, 240x400, 240x320, 240x240, 320x200, 320x240

Display Controller - Block Diagram

Figure 2 depicts the DB9000AXI4 Display Controller IP release supporting baseline display processing features. Contact Digital Blocks. Contact Digital Blocks regarding optional advanced display processing features.

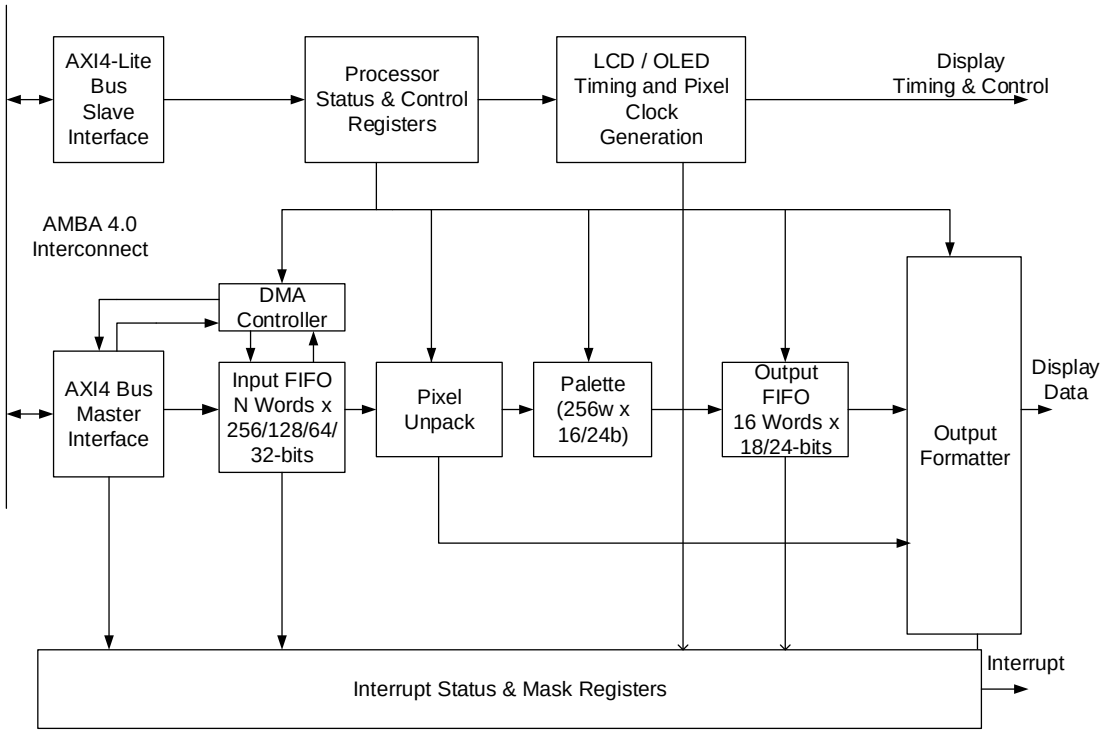

Figure 2: DB9000AXI4 AMBA Interconnect TFT LCD Controller

Verification Method

The DB9000AXI4 contains a simulation test suite with AXI4 Bus functional models that program the DB9000AXI4 control & status registers via the AXI/AHB/APB Slave Bus, generates frame buffer data in response to AXI4 Master requests, and checks expected results.

Customer Evaluation

Digital Blocks offers a variety of methods for prospective customers to evaluate the DB9000AXI4. Please contact Digital Blocks for additional information.

Deliverables

The DB9000AXI4 is available in synthesizable RTL Verilog, along with a simulation test bench with expected results, datasheet, and user manual.

Ordering Information

Please contact Digital Blocks for additional technical, pricing, evaluation, and support information.

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